

# BA01(Q570/H570/B560) Version : 4.1

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## CPU :

**Intel RocketLake-S**

## System Chipset :

**Intel RocketLake Chipset**

## On Board Chipset :

**IMVP8 -- NCP81220 4+2 Phase**  
**Gigabit LAN -- INTEL-I219LM Co-LAY RTL8111K**  
**HDA Codec -- Realtek ALC623**  
**Super I/O --NCT6686D-L**  
**SPI Flash 256Mb +128Mb**

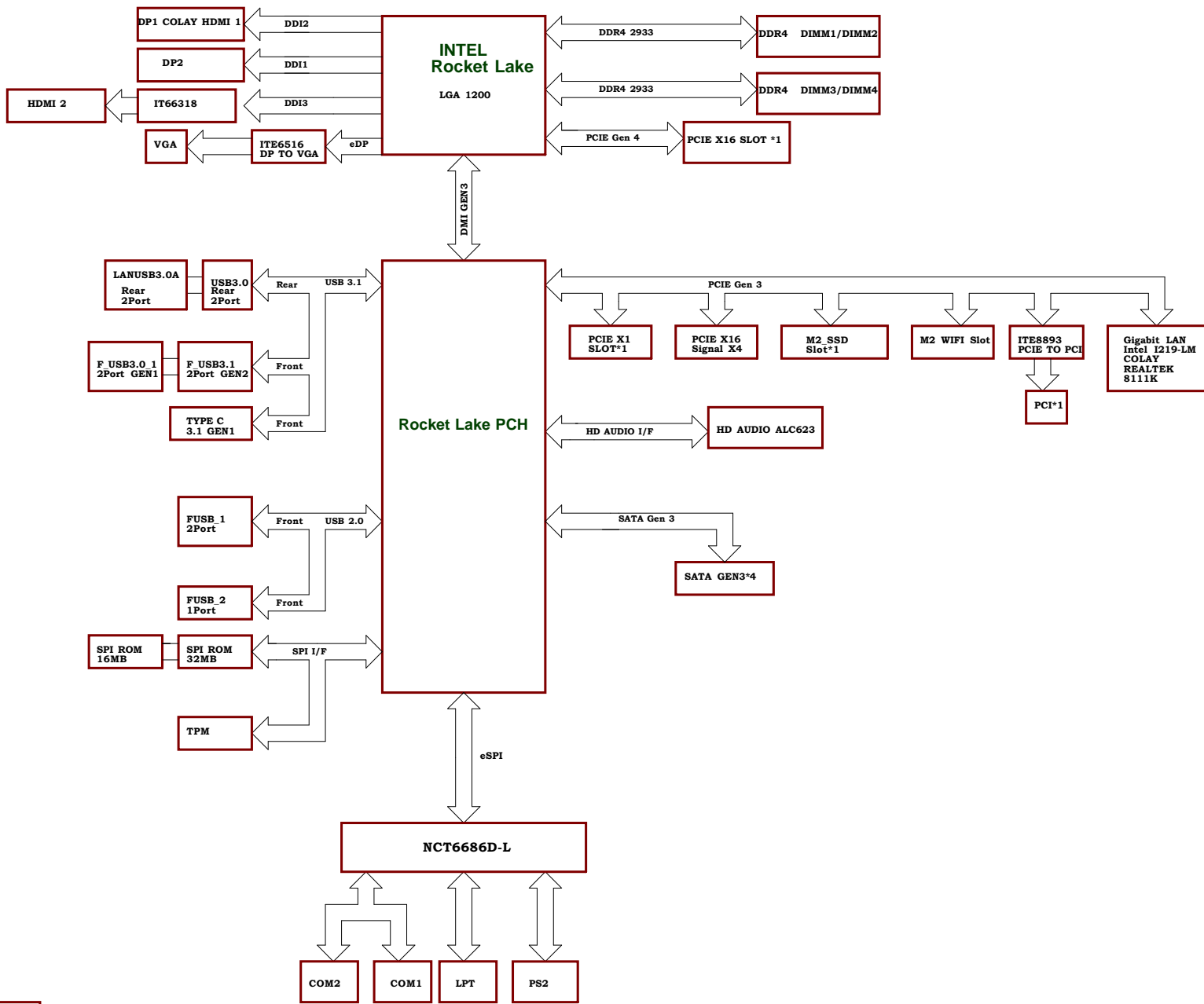
## Main Memory :

**2 Channel DDR 4 \* 4 (Max 128GB)**

## Expansion Slot :

**PCI Express x16 Slot \* 1**  
**PCI Express x4 Slot \* 1**  
**PCI Express x1 Slot \* 1**  
**PCI SLOT \* 1**

**lenovo**



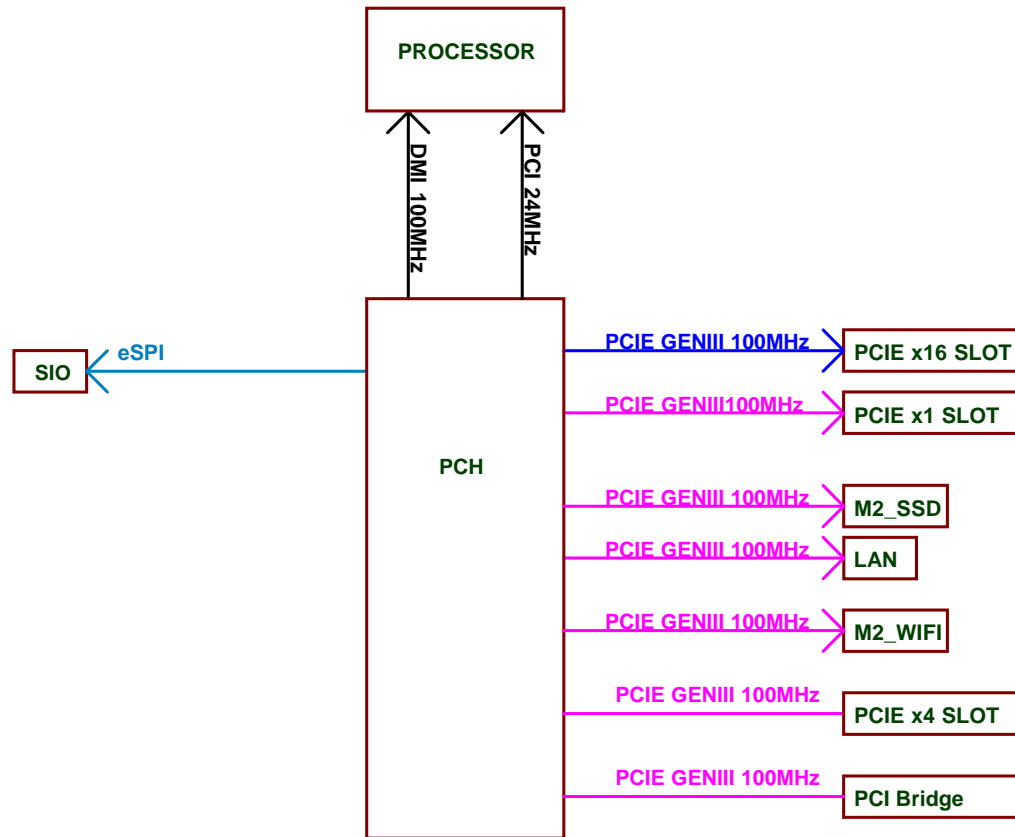
Slot Sequence:

PCIE X16

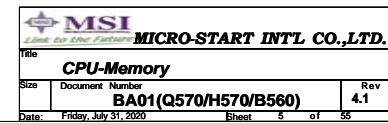
PCIE X1

PCIE X16(signal x4)

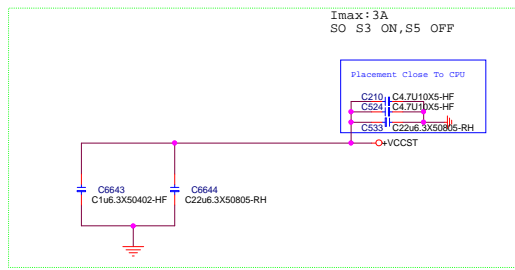
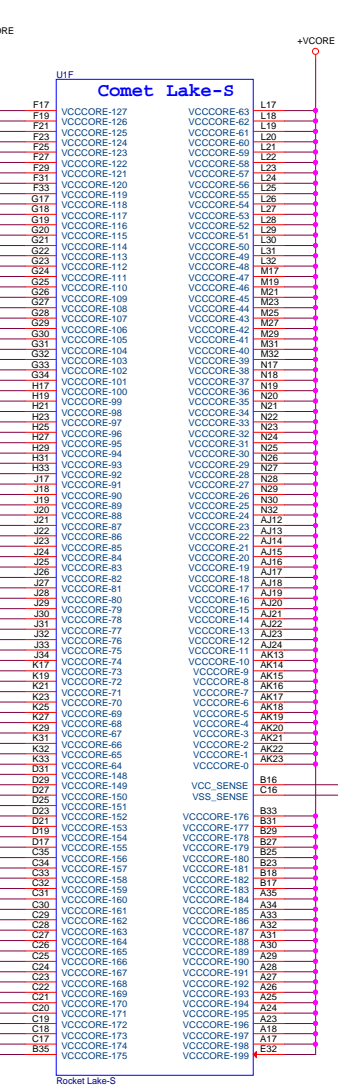
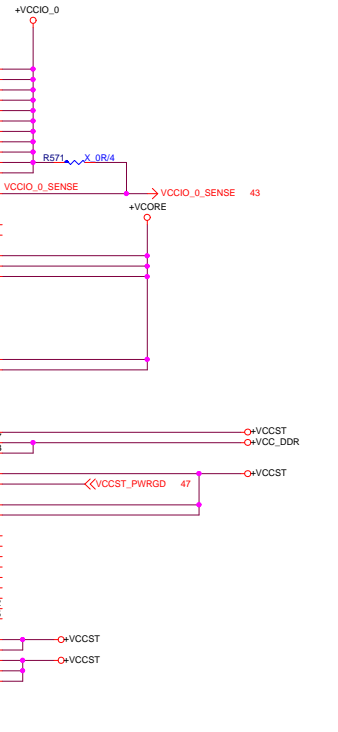
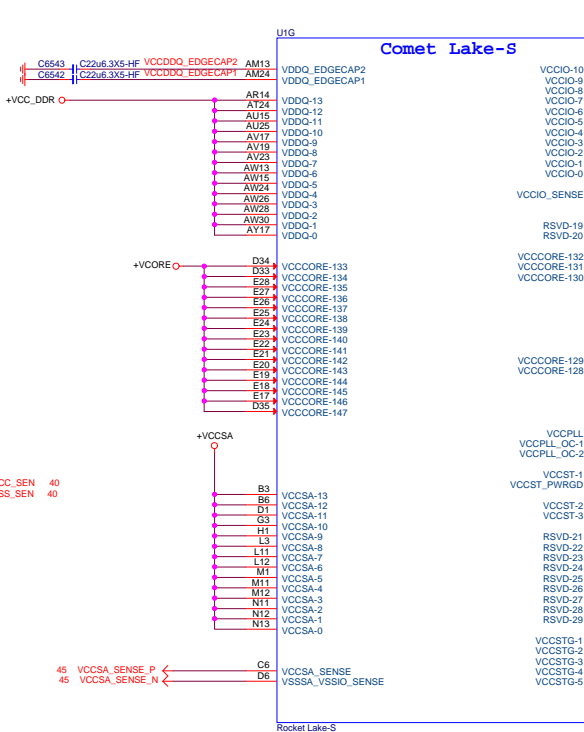
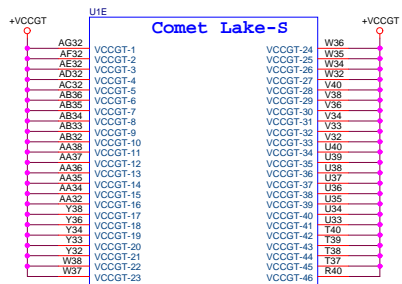
PCI SLOT

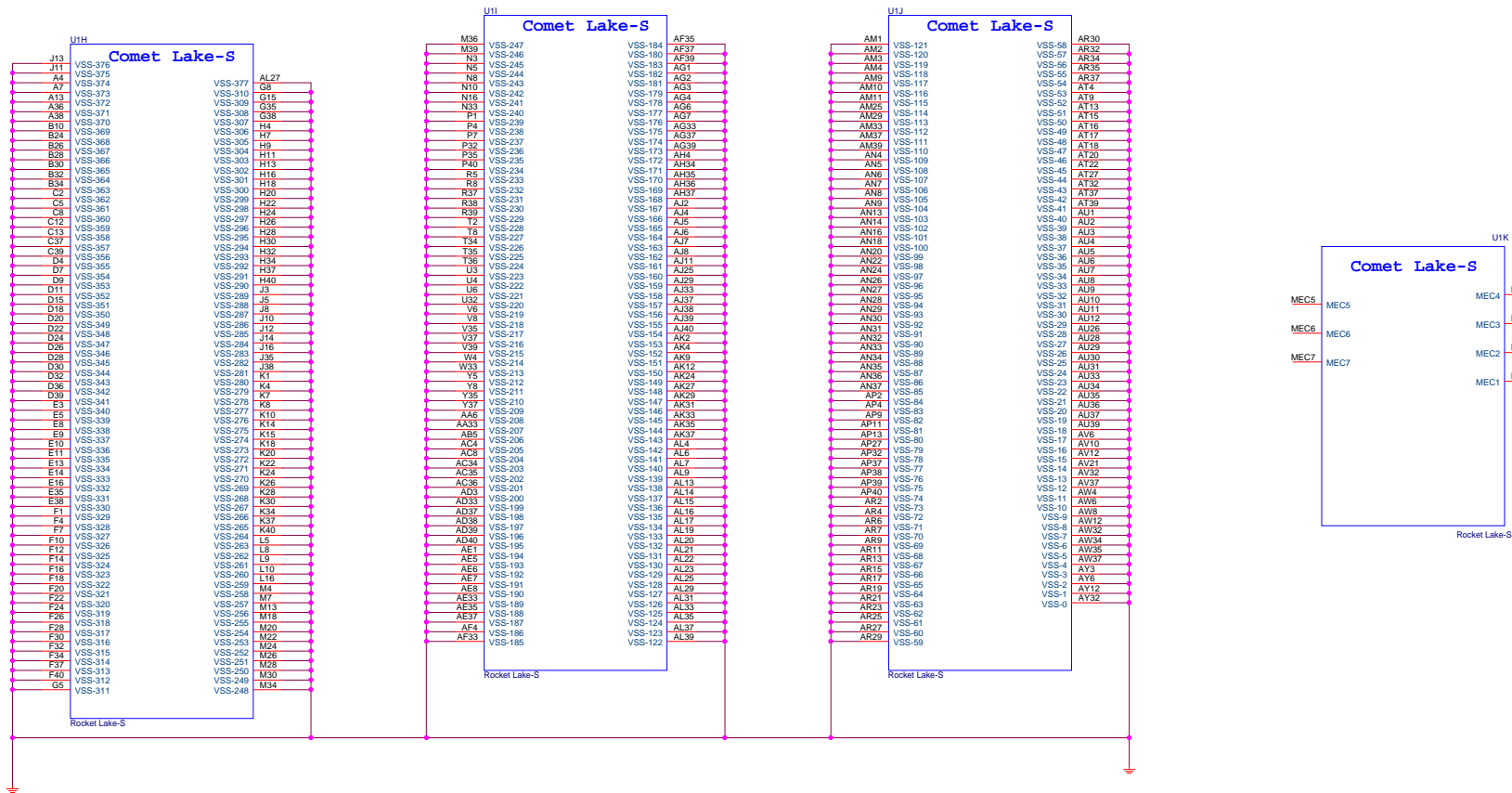




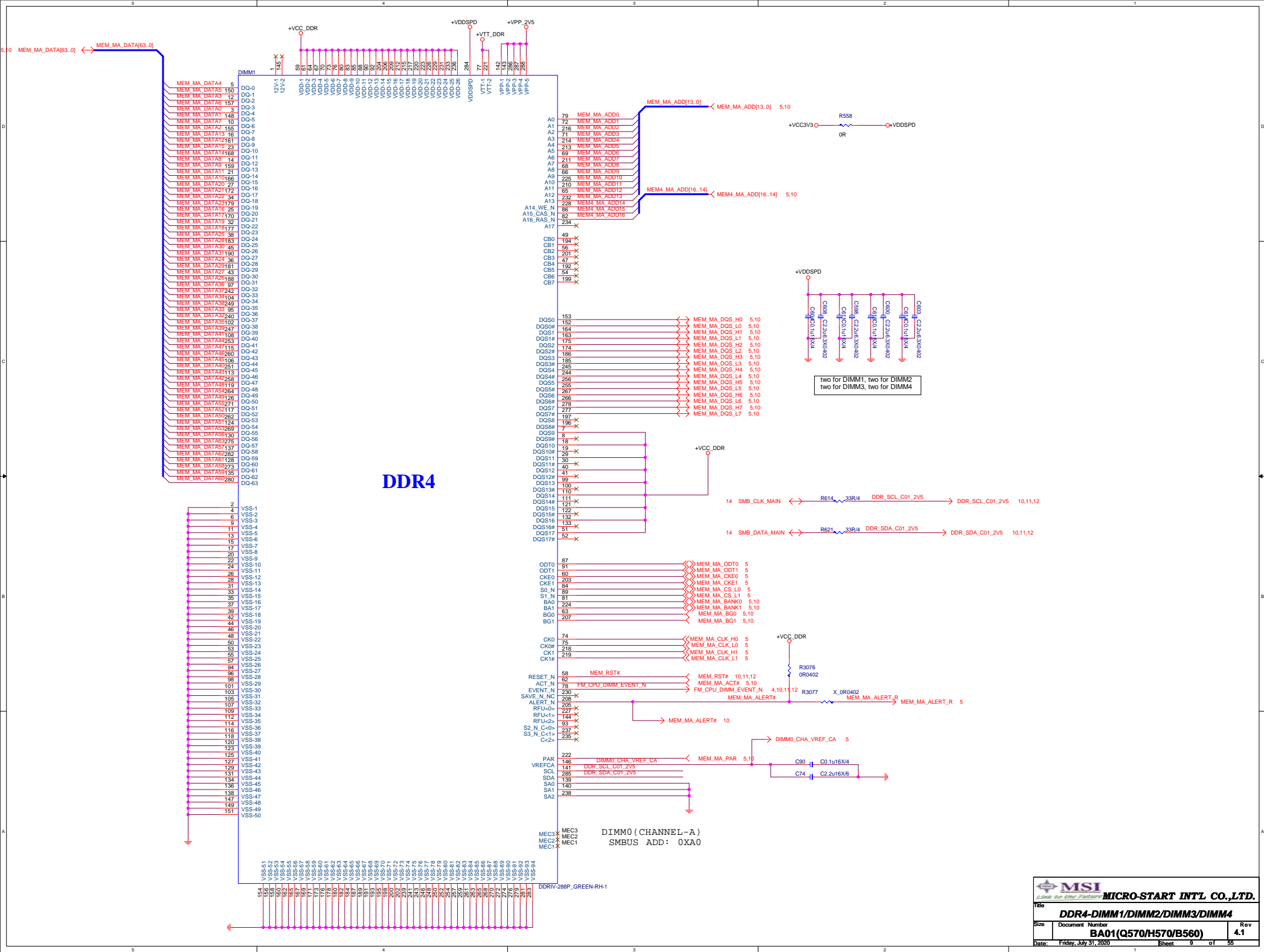


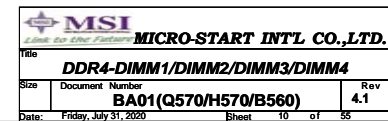


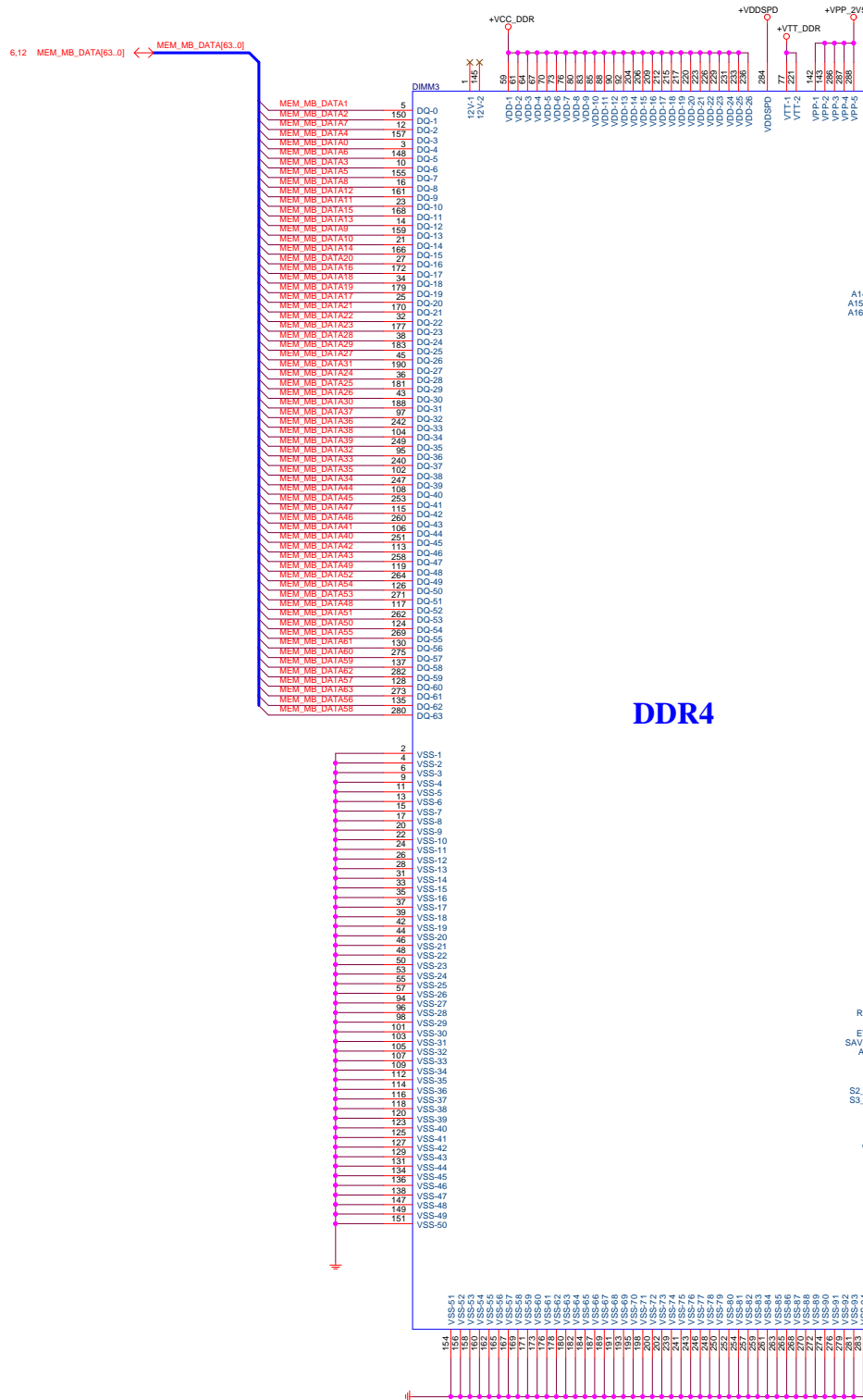


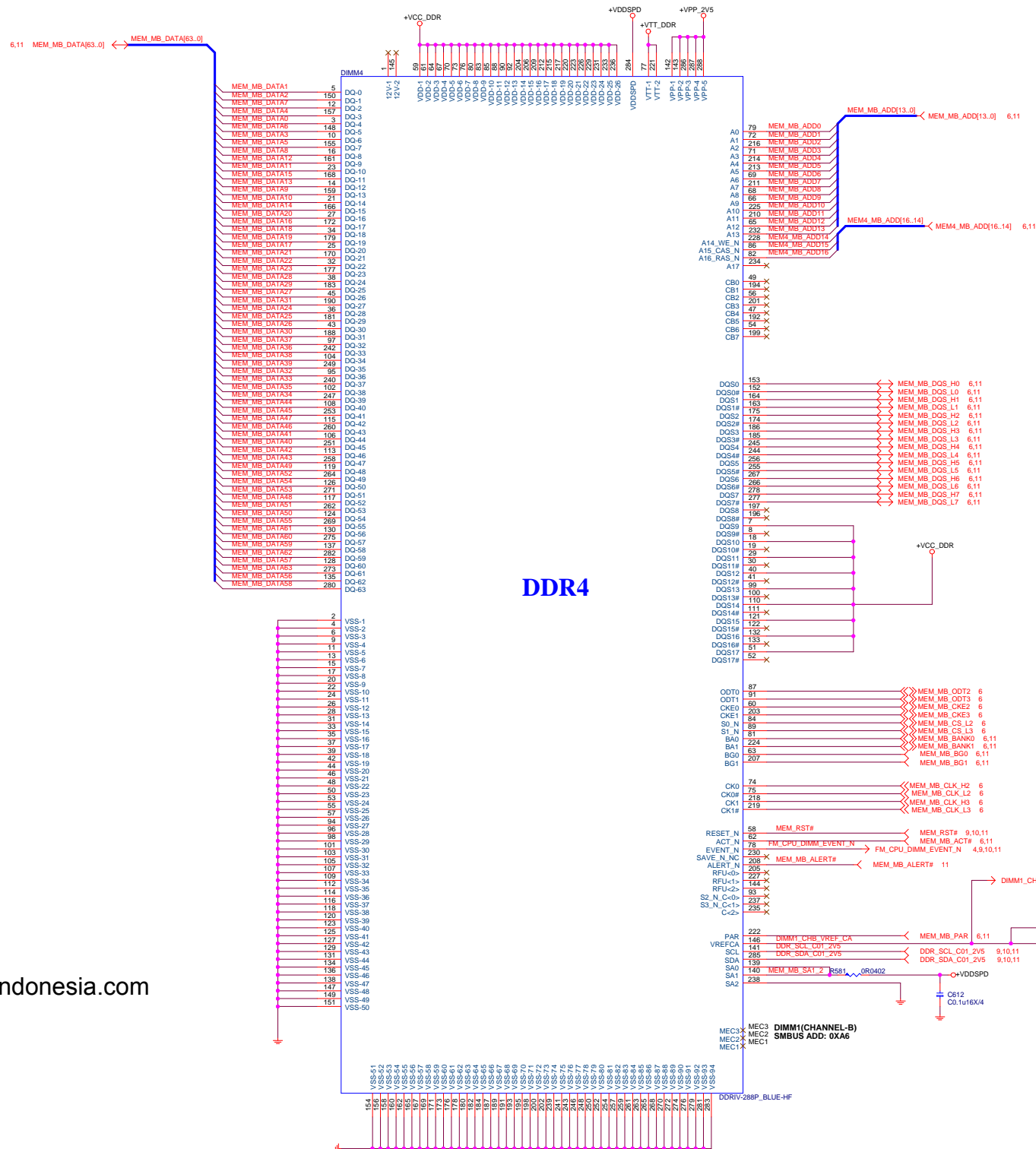




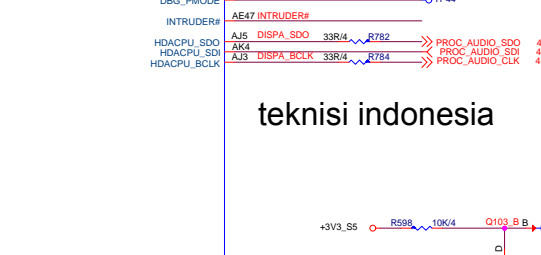
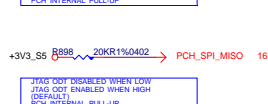
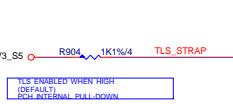
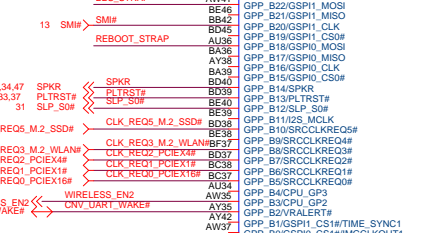
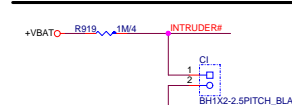
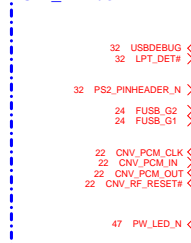




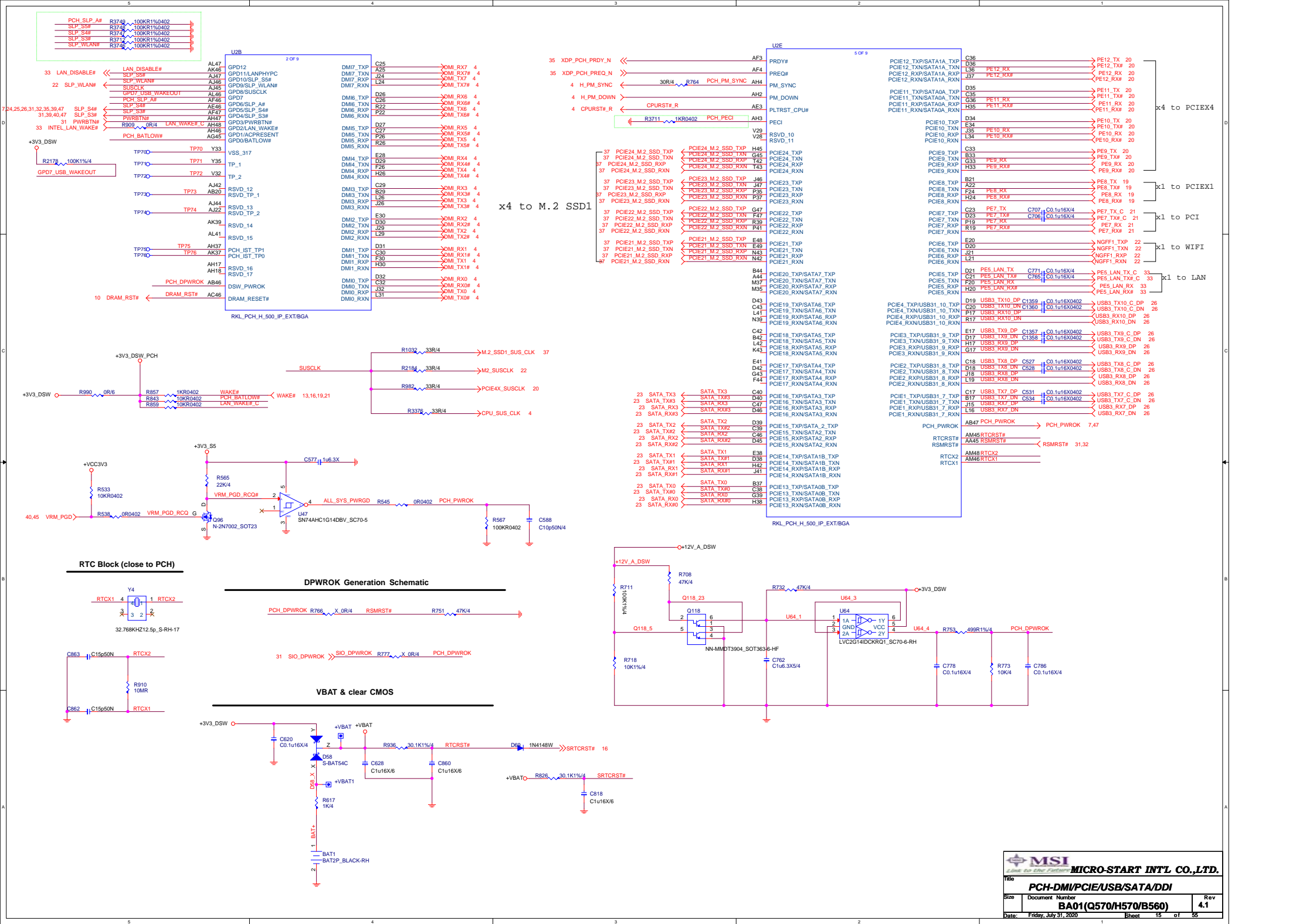


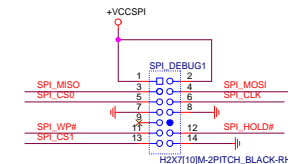
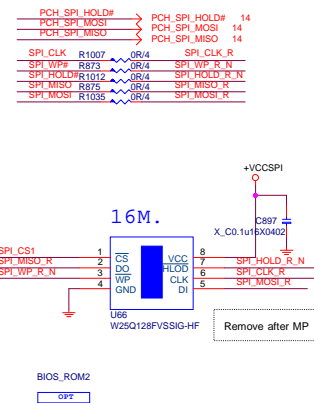
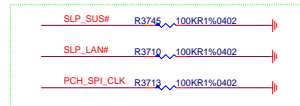
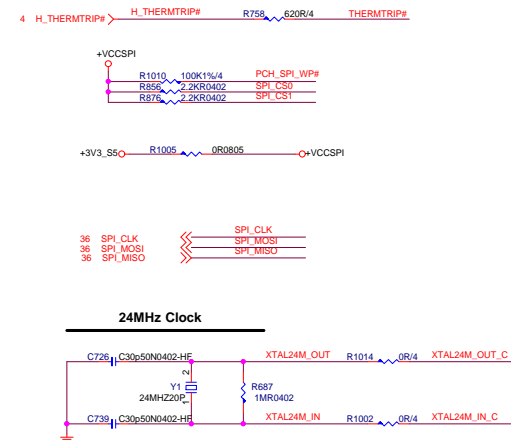




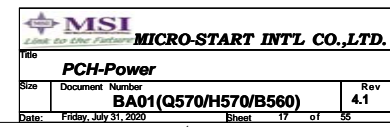


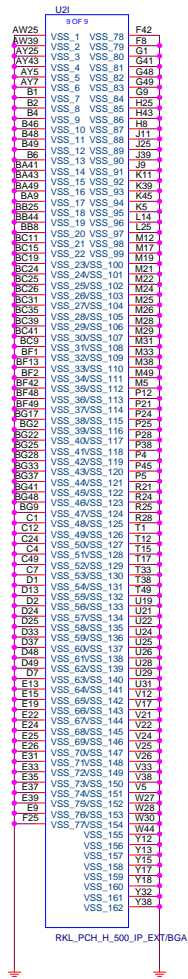
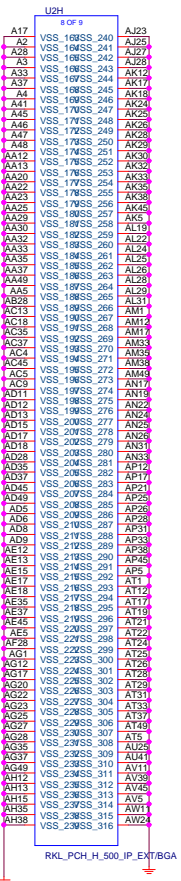




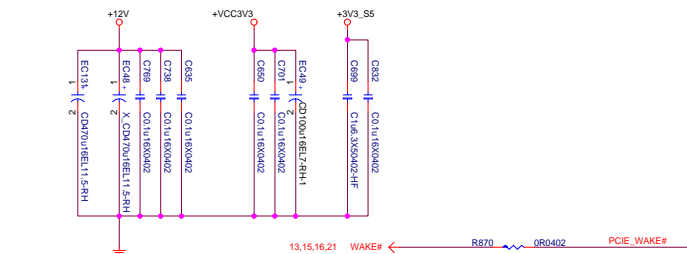




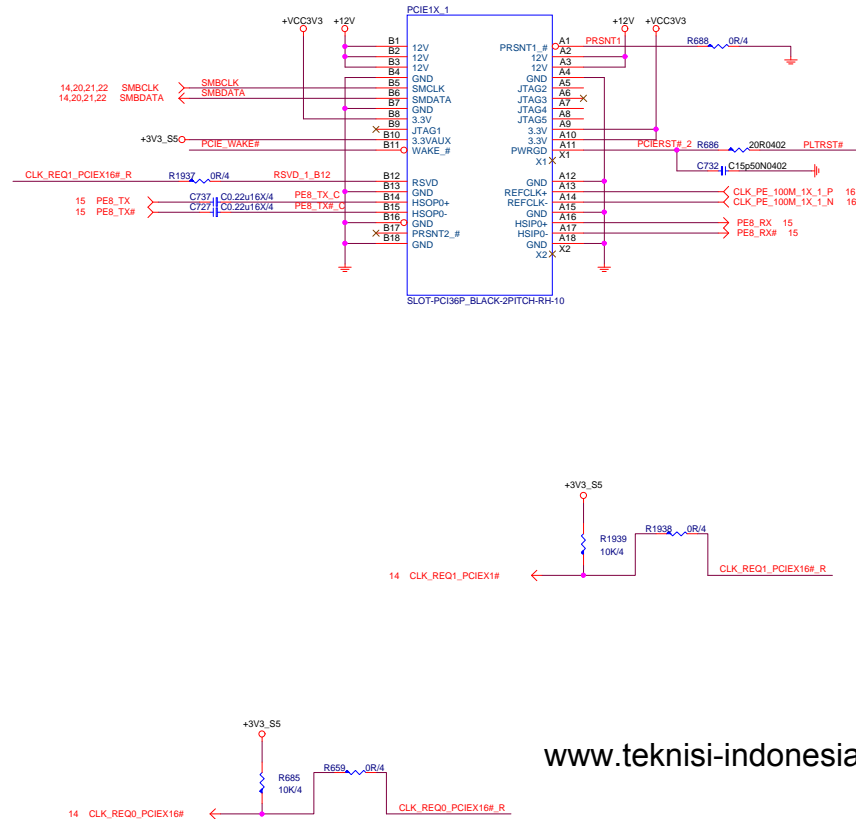




## PCI EXPRESS X16 SLOT

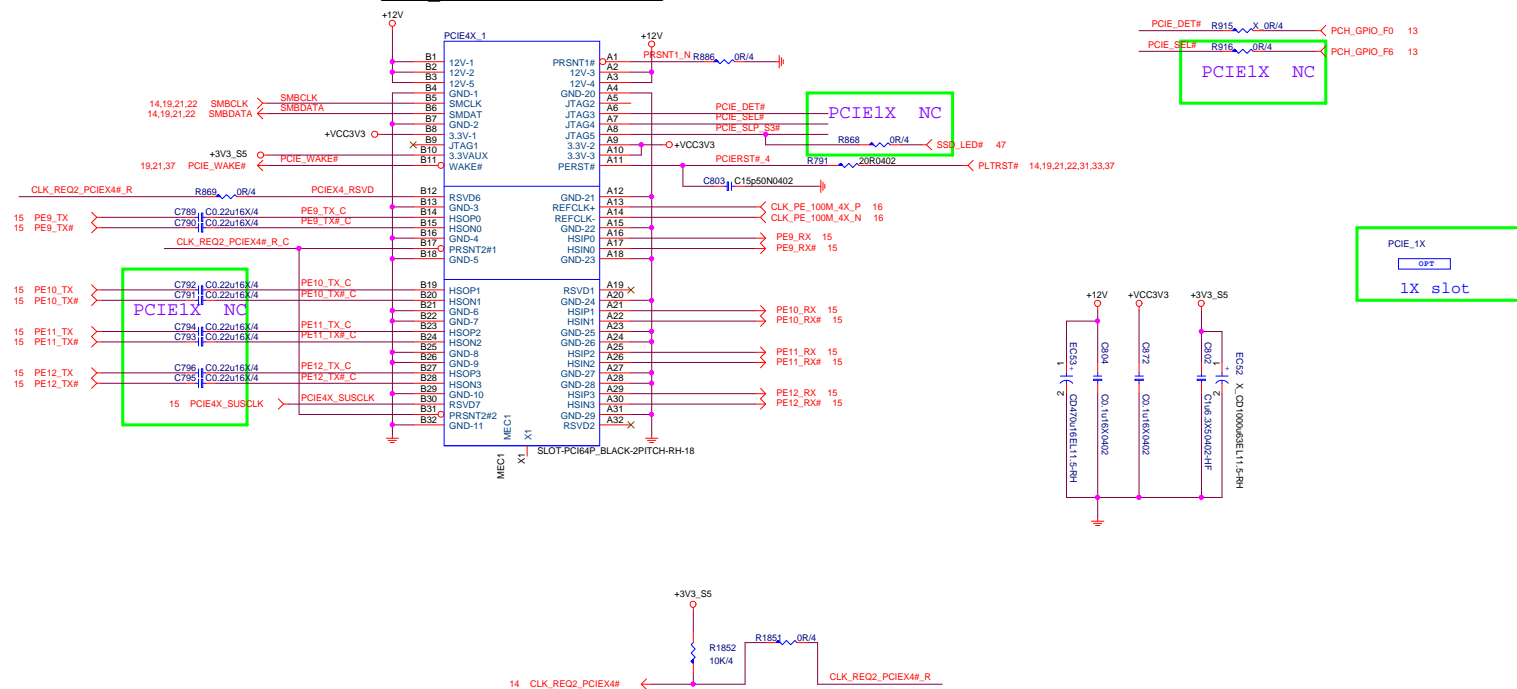


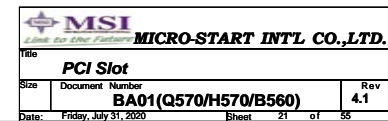
## PCI EXPRESS x1-PORT



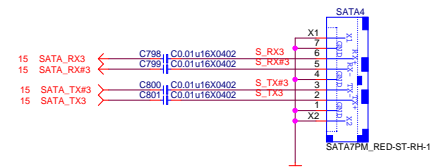
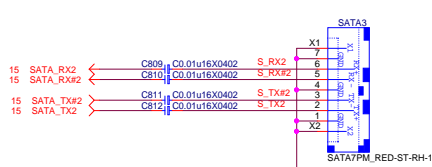
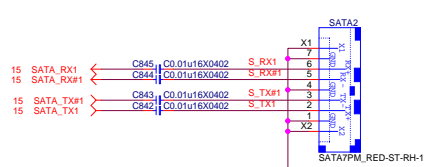
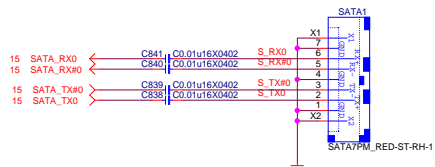
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# PCI EXPRESS X4 SLOT

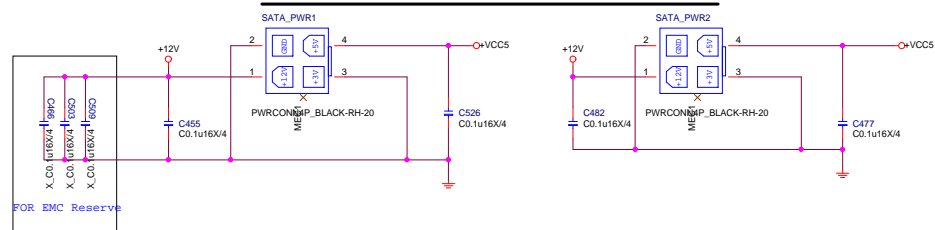




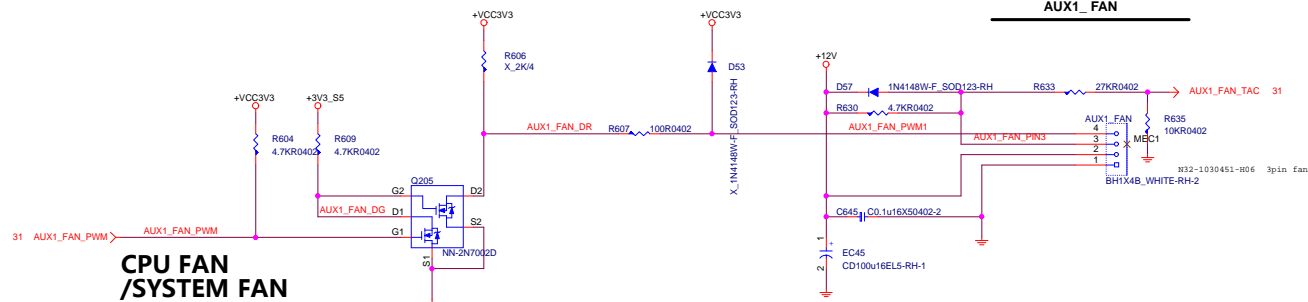




## SATA Power Output Connector

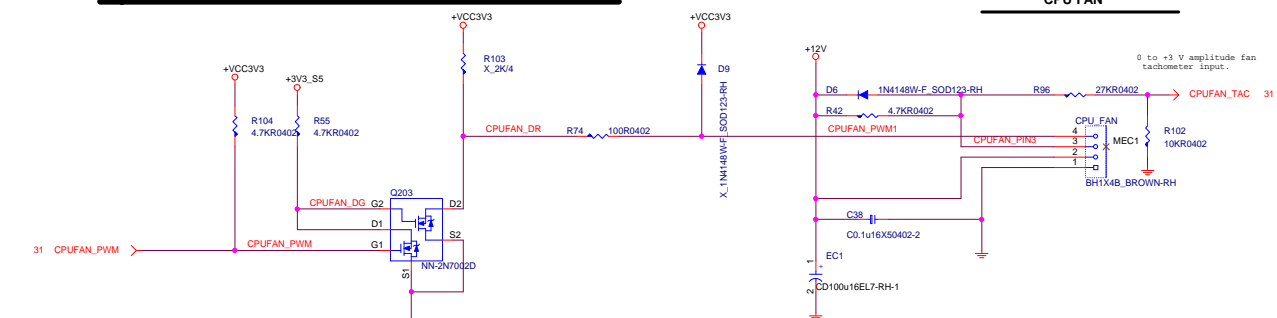


## AUX1\_FAN

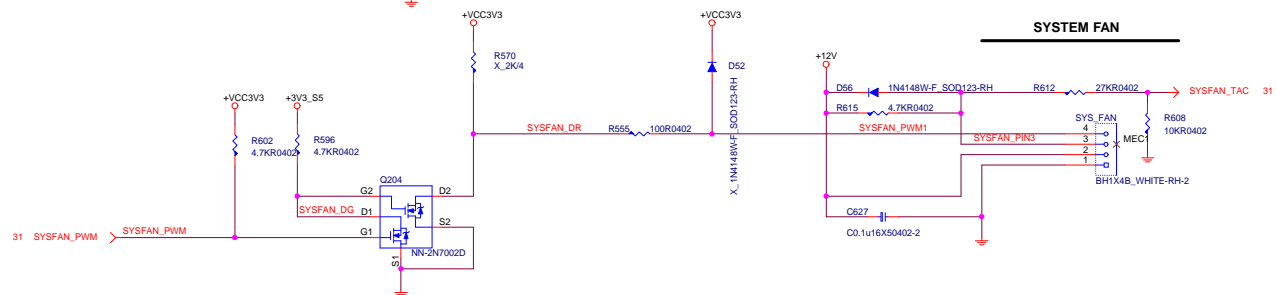


## CPU FAN /SYSTEM FAN /POWER FAN

## CPU FAN

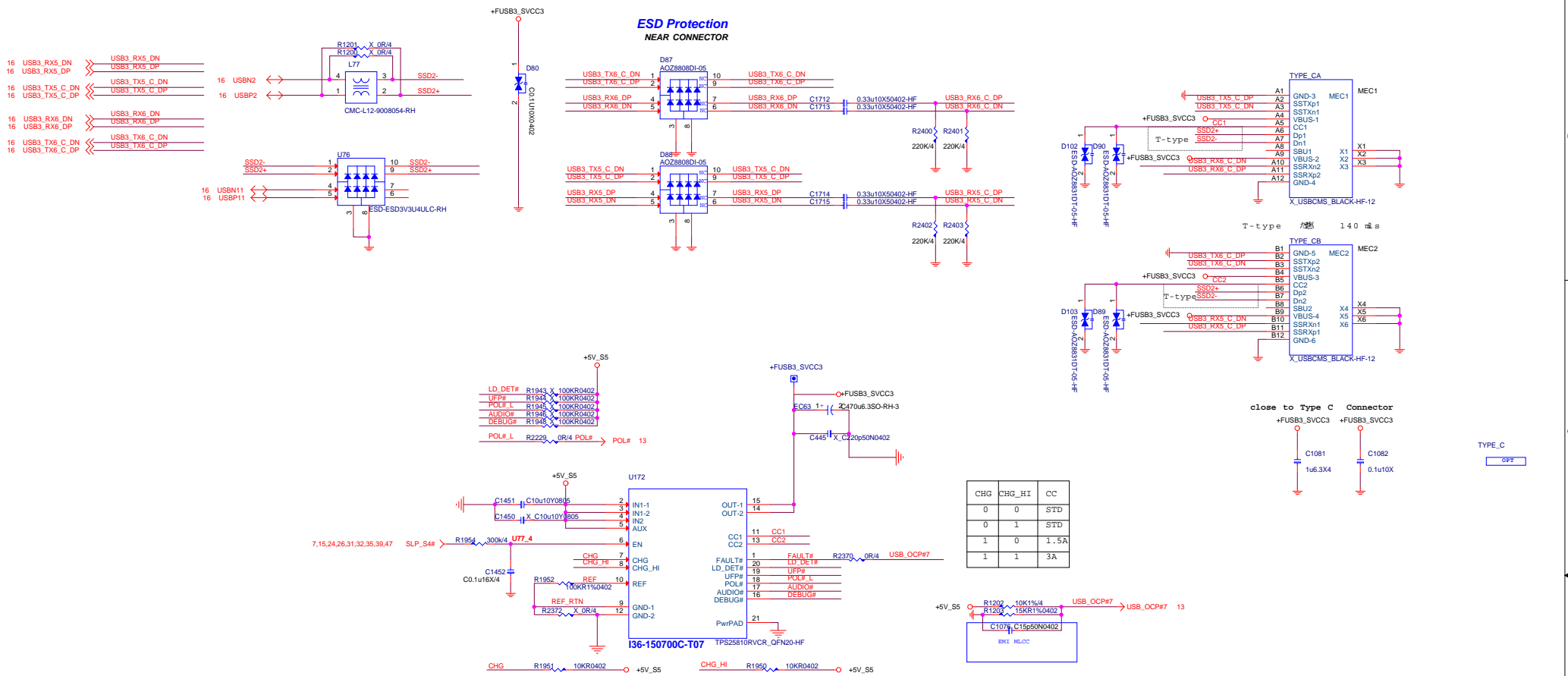


## SYSTEM FAN

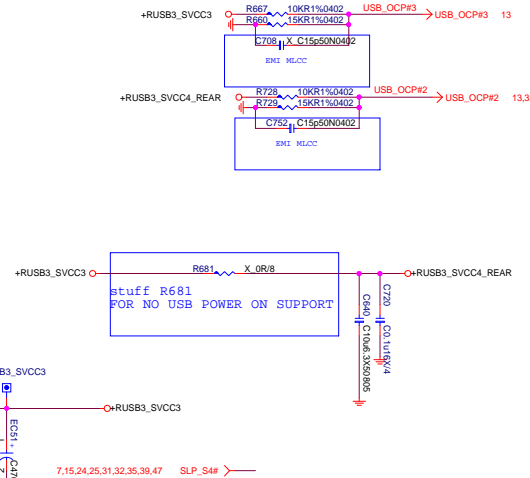
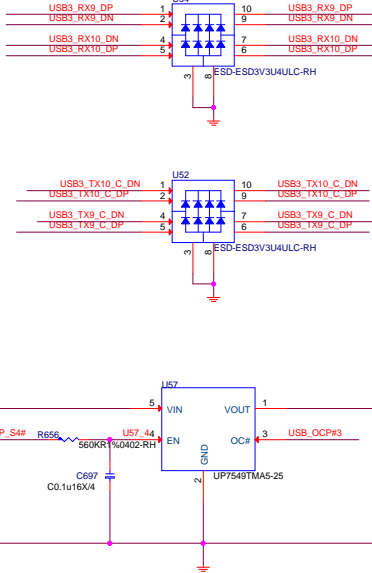
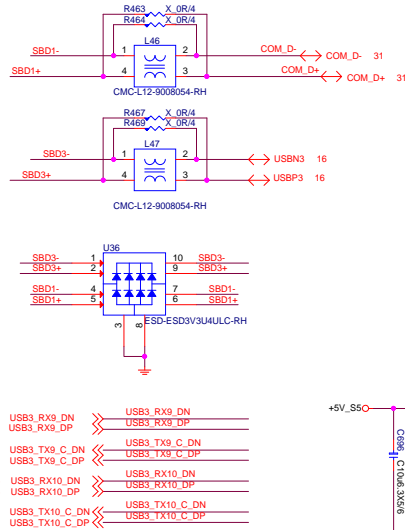
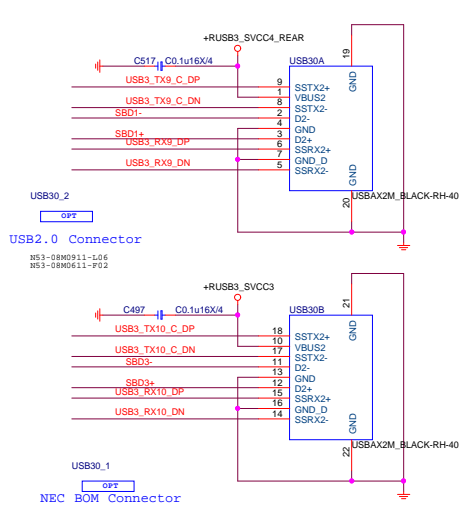




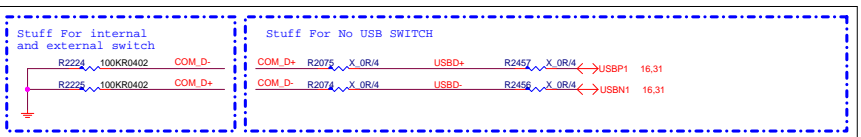
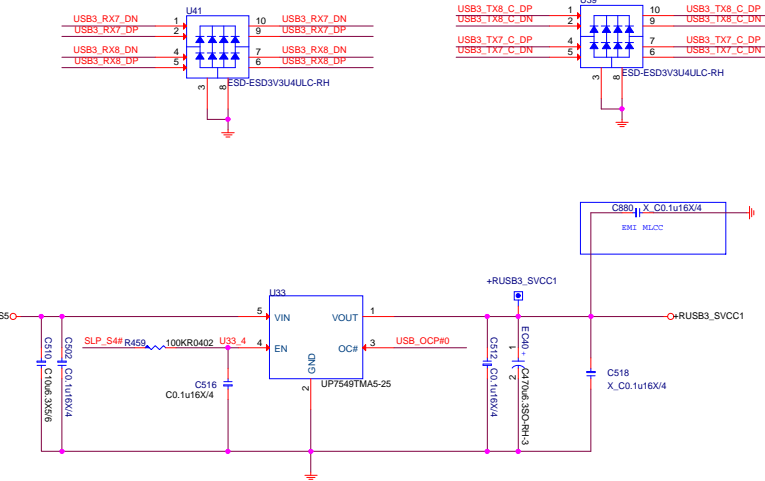
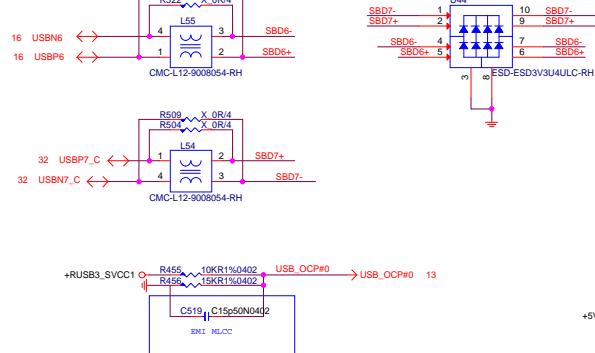
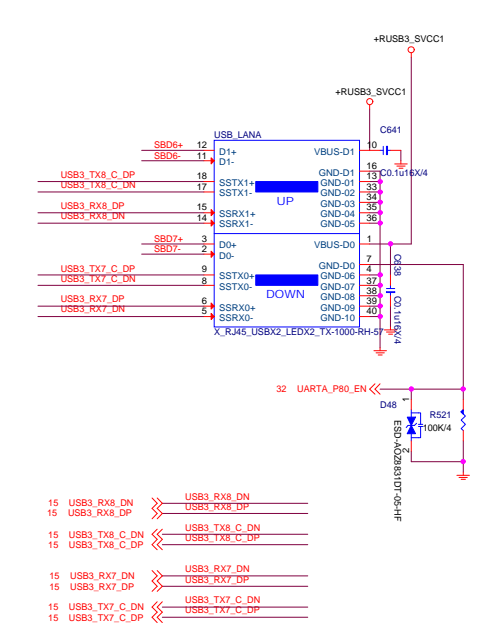




# Rear IO USB Connector For USB Port 7/8

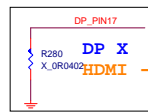
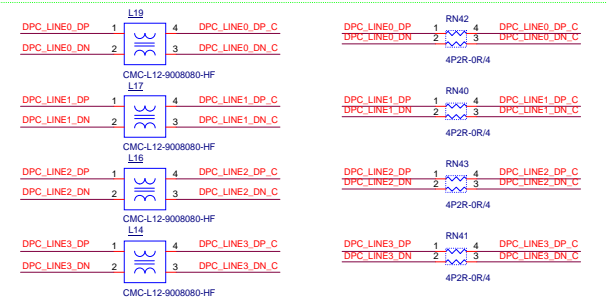
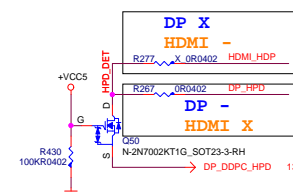
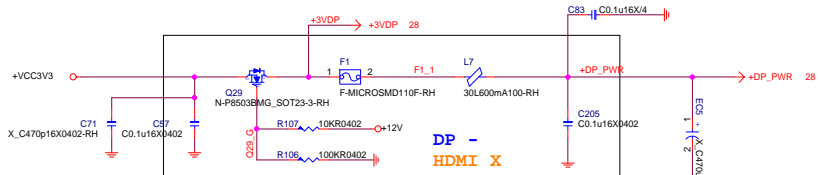
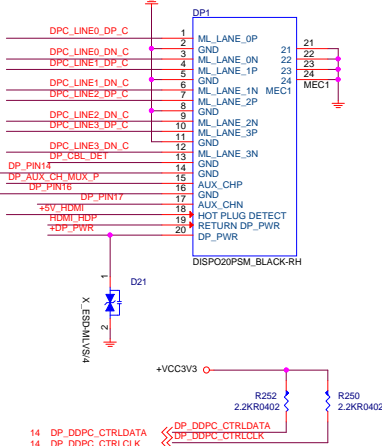
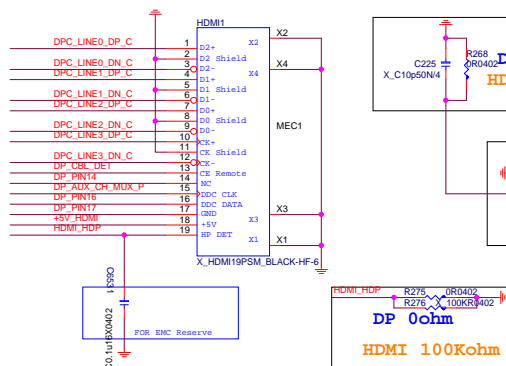
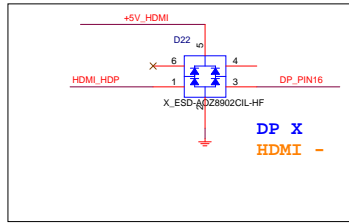
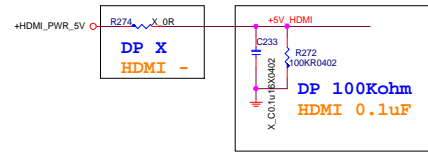
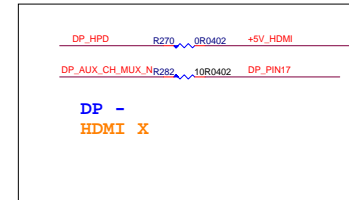
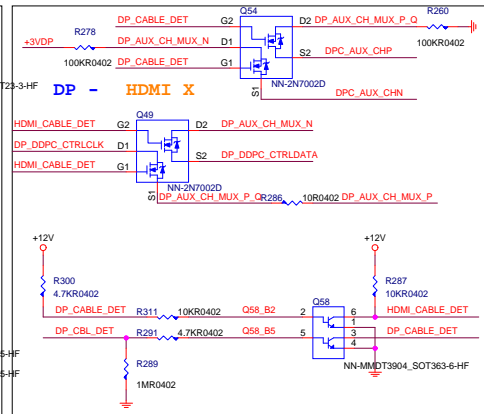
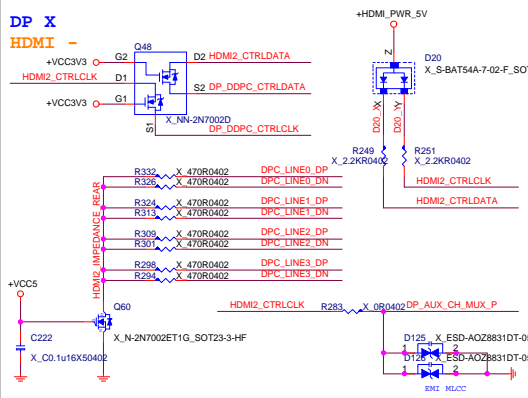
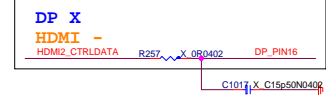
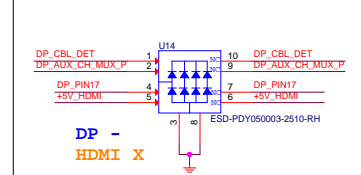
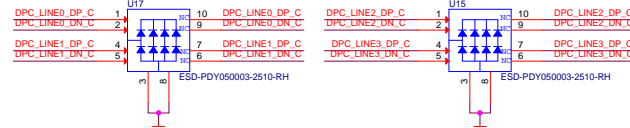
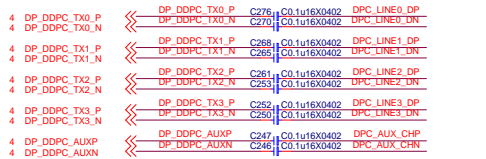


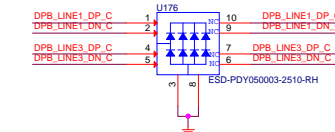
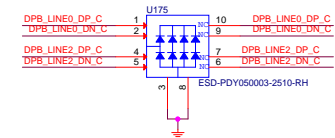
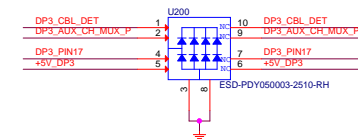
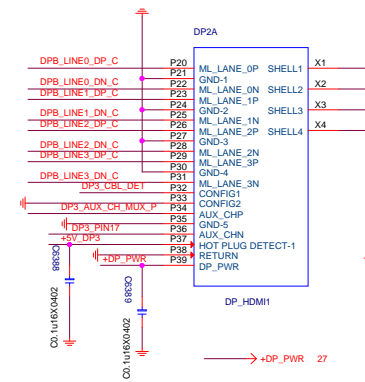
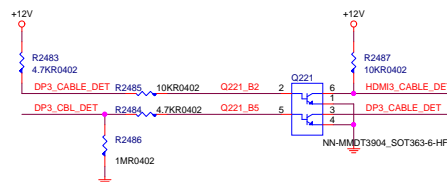
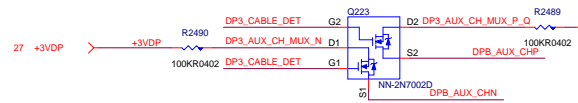
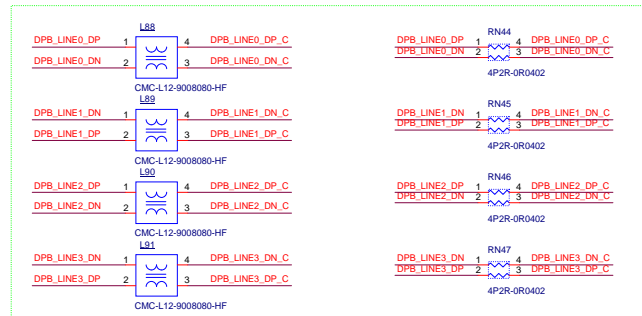
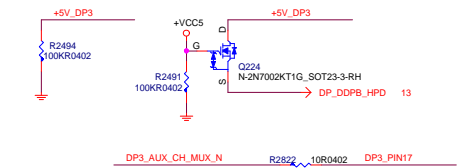
# Rear USB Connector For USB Port 9 / 10




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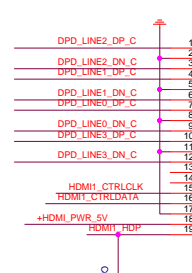
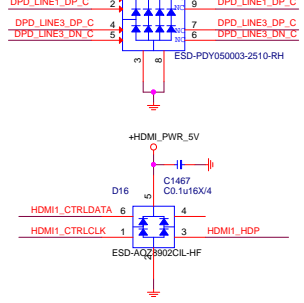
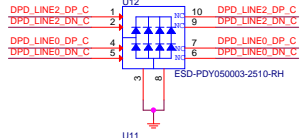
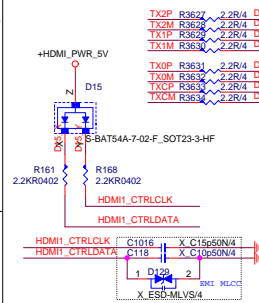
## DP1 Co-lay HDMI1 CONN



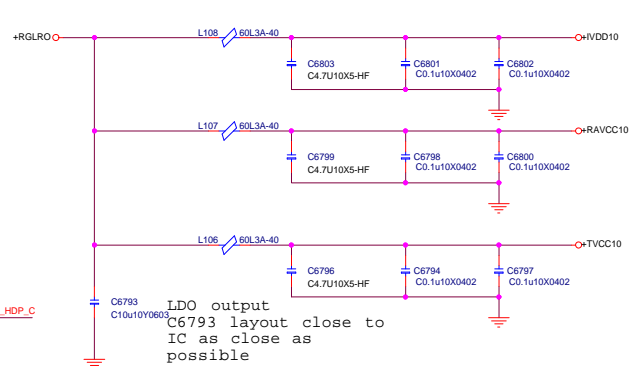
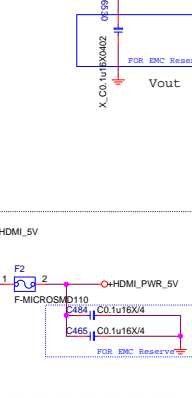


 <b>MSI</b> <i>Look to the Future</i>				<b>MICRO-START INT'L CO.,LTD.</b>			
<b>Title</b> <b>Display Port/HDMI Port</b>							
<b>Size</b>		<b>Document Number</b> <b>BA01(Q570/H570/B560)</b>				<b>Rev</b> <b>4.1</b>	
<b>Date:</b> Friday, July 31, 2020		<b>Sheet</b> 28		<b>of</b> 55			

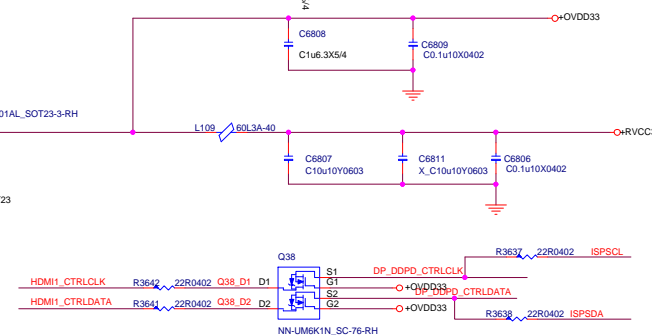
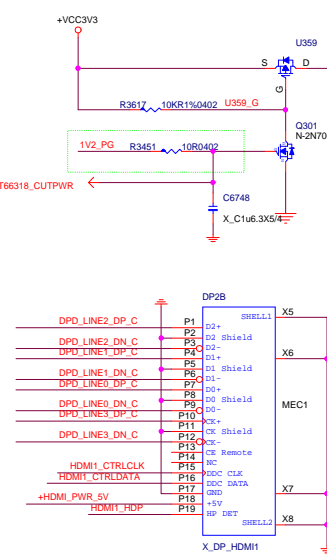
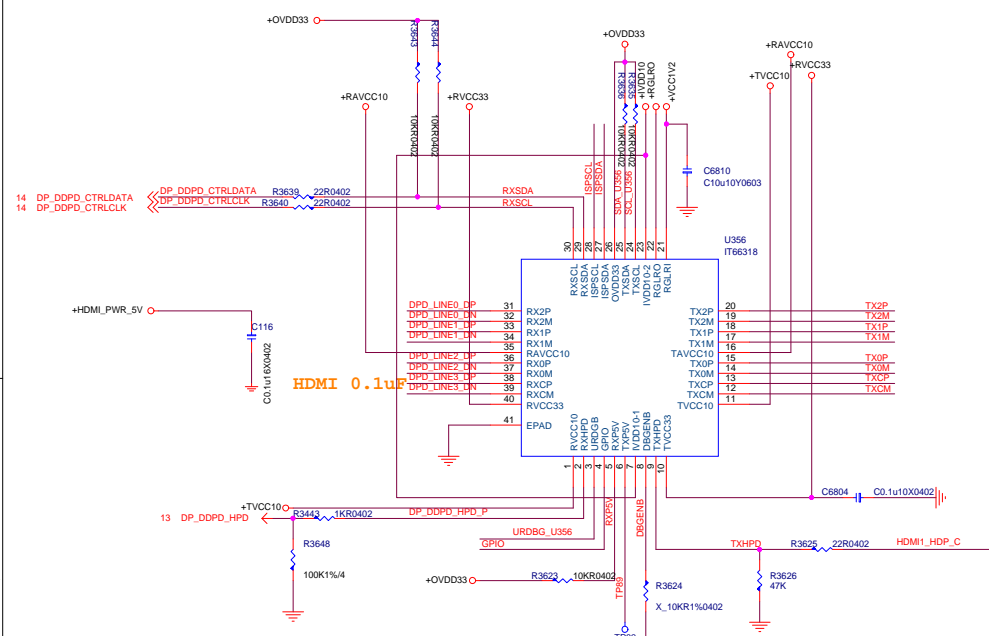
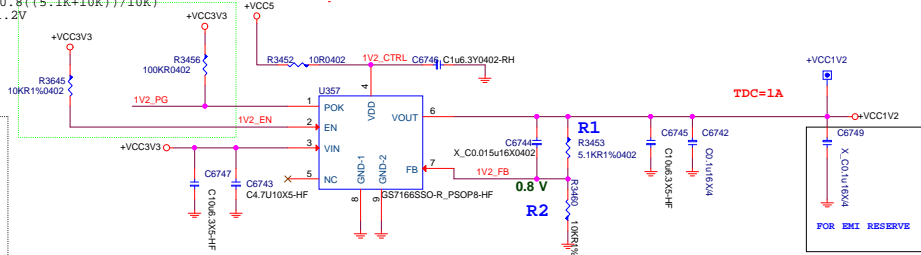
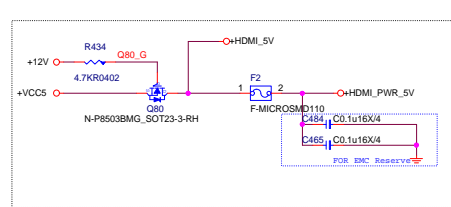
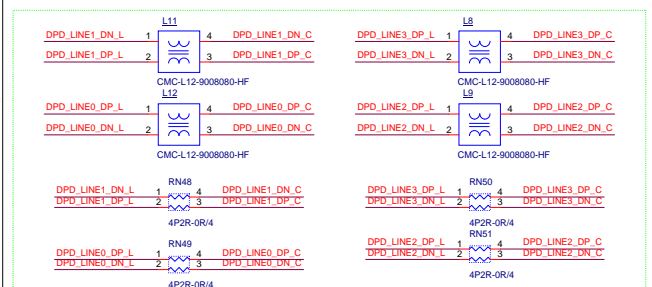
DP_DDPD_TX0_P	C196	C0.1u16X0402	DPD_LINE0_DP
DP_DDPD_TX0_N	C197	C0.1u16X0402	DPD_LINE0_DN
DP_DDPD_TX1_P	C187	C0.1u16X0402	DPD_LINE1_DP
DP_DDPD_TX1_N	C178	C0.1u16X0402	DPD_LINE1_DN
DP_DDPD_TX2_P	C169	C0.1u16X0402	DPD_LINE2_DP
DP_DDPD_TX2_N	C164	C0.1u16X0402	DPD_LINE2_DN
DP_DDPD_TX3_P	C159	C0.1u16X0402	DPD_LINE3_DP
DP_DDPD_TX3_N	C150	C0.1u16X0402	DPD_LINE3_DN



$$\begin{aligned} V_{out} &= 0.8[(R1+R2)/R2] \\ &= 0.8[(5.1K+10K)/(10K)] \\ &= 1.2V \end{aligned}$$

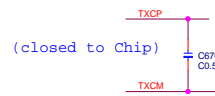


LDO output  
C6793 layout close to  
IC as close as  
possible

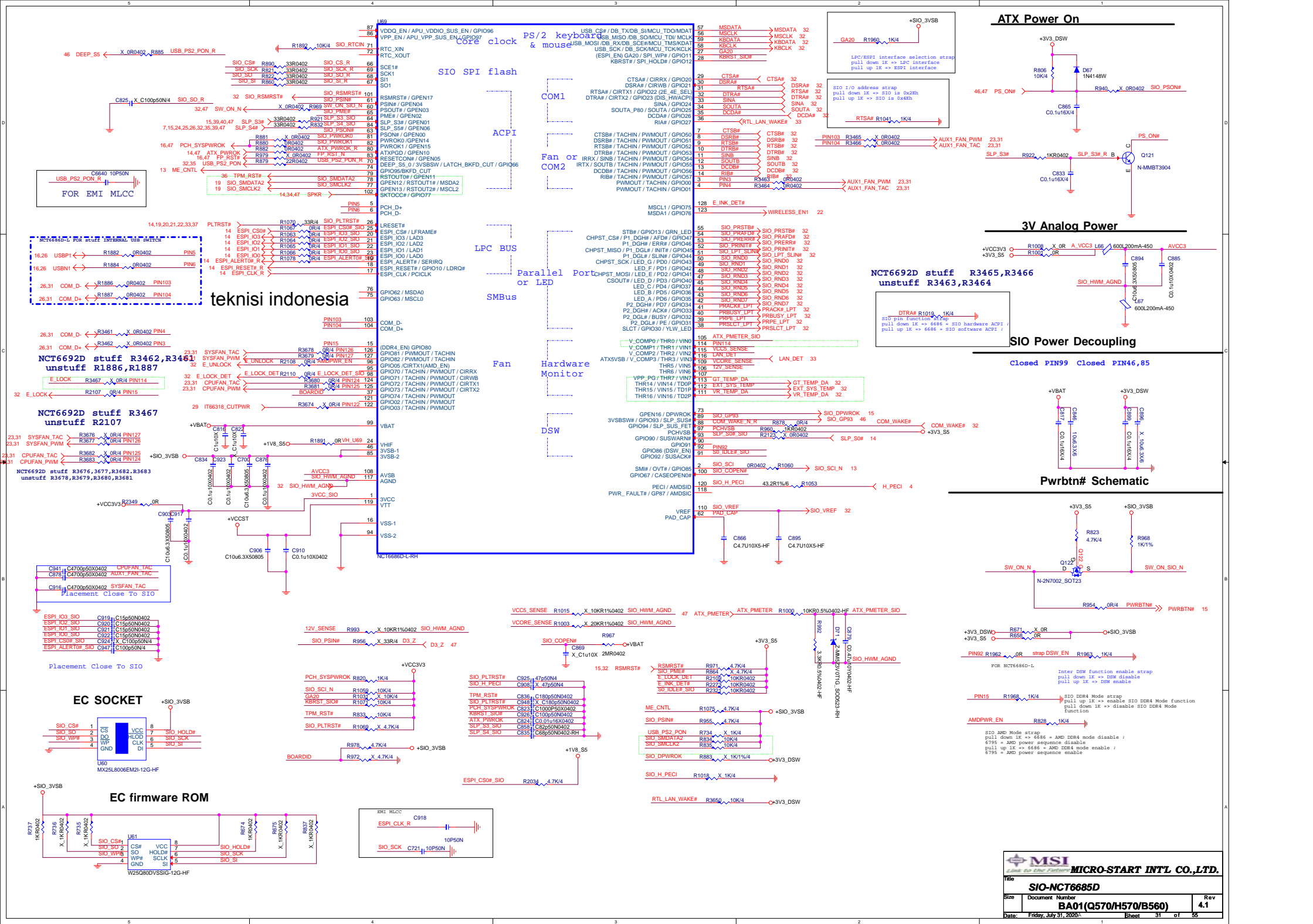


Output Swing	GPIO	URDBG
Level 1 (Lowest)	0	0
Level 2 (Default)	0	1
Level 3	1	0
Level 4 (Highest)	1	1

Output Swing	GPIO	URDBG
Level 1 (Lowest)	0	0
Level 2 (Default)	0	1
Level 3	1	0
Level 4 (Highest)	1	1









The diagram illustrates the internal circuitry of a USB to PS2 adapter. It is divided into three main functional blocks:

- USB to PS2 Conversion:** This section shows the connection between a USB interface (C136, C0.1uF, X0402) and a PS2 interface (KB\_MS). It includes signal lines for MS\_DATA, MS\_CLK, KB\_DATA, and KB\_CLK, along with power supply connections (+RUSB\_VCC\_PS2, +RUSB\_VCC\_PS2).
- EMI solution:** This block focuses on electromagnetic interference (EMI) mitigation. It features a network of capacitors (R134, R151, R164, R174) and inductors (FB1, FB2, FB3, FB4) connected to the PS2 signals and ground to filter out noise.
- ESD protection:** This section shows the protection against electrostatic discharge (ESD). It includes a diode (D1) and a capacitor (C137) connected to the PS2 signals and ground to protect the circuit from voltage spikes.

Support PS2 power on for (SKU NEC)

**SIO GPIO66**  
**S0/S3: output 1**  
**Deep S5: PS2 power on EN, output 1**  
**Deep S5: PS2 power on DIS, output 0**

[illegible][illegible]

**E-LOCK Pin Header**

1. 12V always power/1.5A Max  
 2. Control @0V lock(can work under system power off)  
 3. Detect(always power pull high)  
 4. GND  
 5. Control @1V unlock(can work under system power off)

Chassis Type

	CHASSIS_ID1 (PCH GPIO3)	CHASSIS_ID2 (PCH GPIO3)
25L(Default)	1	1
31L	0	0
20L	0	1
11L	0	0

31 E\_LOCK\_DET ← E-LOCK\_DET  
 31 E\_UNLOCK ← E-UNLOCK

SOLENOID\_HED 1 2  
 1 2  
 3 4  
 5

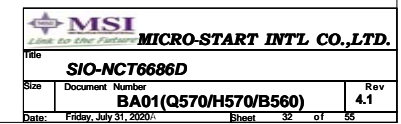
HZX3@M\_RED-RH

EXT\_SYS\_TEMP SENSE\_P3 CHASSIS\_ID1 CHASSIS\_ID2

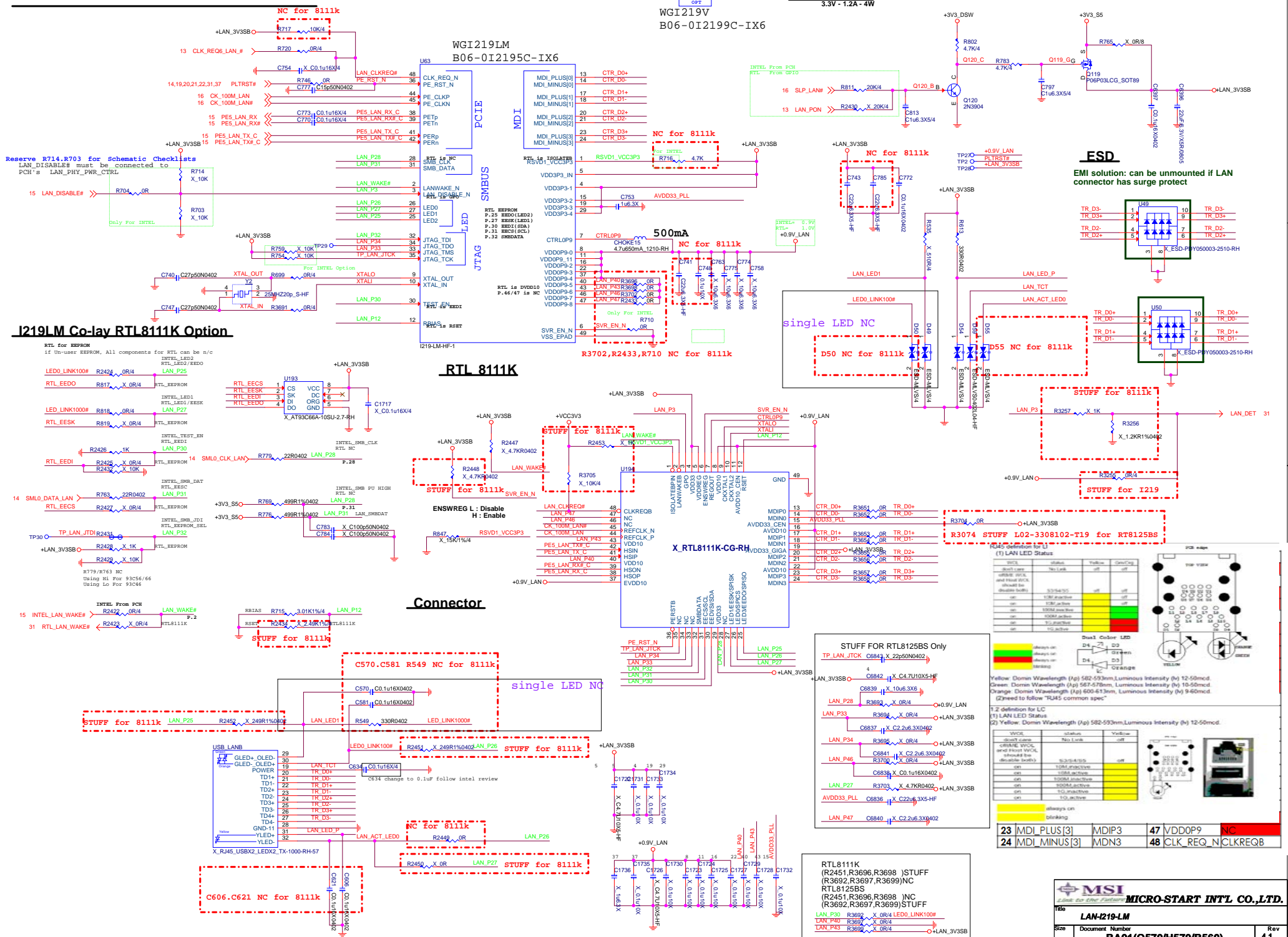
31 SIO\_LPT\_SLN# SIO\_LPT\_SLN1# RN23 2  
 31 SIO\_PRINT# SIO\_PRINT# 6  
 31 SIO\_PERR# SIO\_PERR# 6  
 31 SIO\_PRAFD# SIO\_PRAFD# 8

8P4R-2.7KR0402  
 SIO\_PRSTB# R1050 2.7KR0402

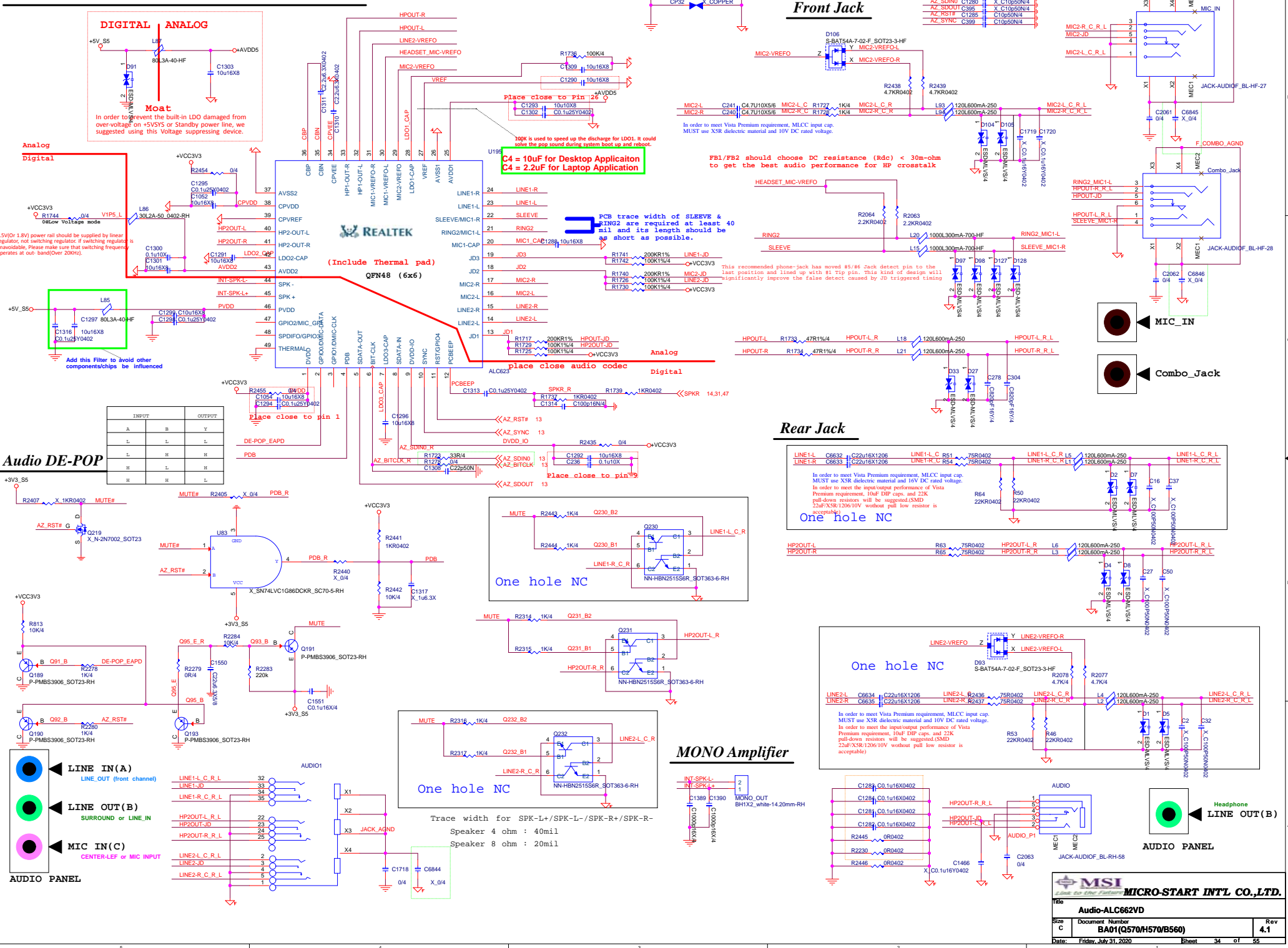
C909  
 C0 102Y0402-RH





**INTEL-I219LM Co-LAY RTL8111K/RTL8125BS**

## Azalia Codec - ALC623

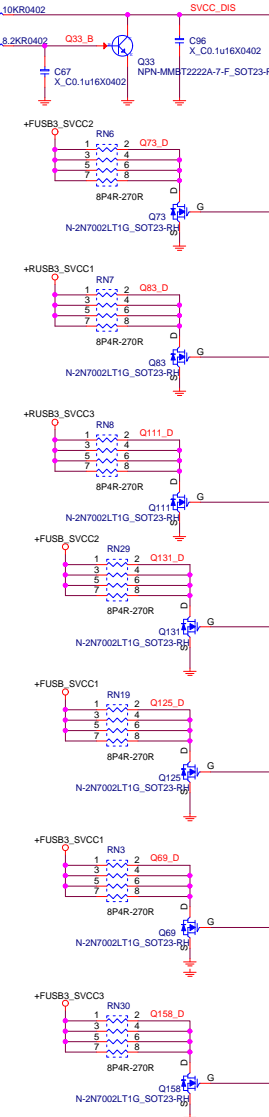
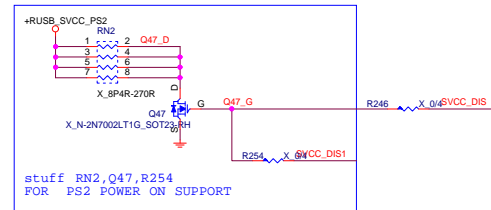
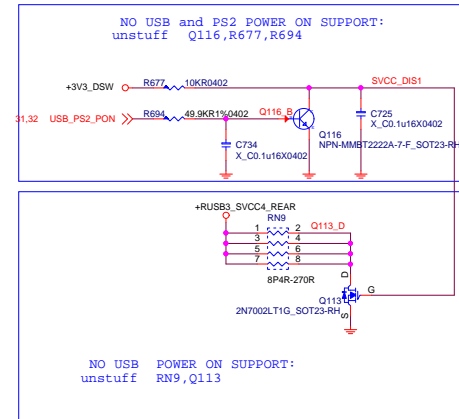


XDP\_CPU\_PREQ# >>> XDP\_CPU\_PREQ# 4  
 XDP\_CPU\_PRDY# >>> XDP\_CPU\_PRDY# 4  
 CPU\_TCK >>> CPU\_TCK 4  
 CPU\_TDO >>> CPU\_TDO 4  
 CPU\_TDI >>> CPU\_TDI 4  
 CPU\_TMS >>> CPU\_TMS 4

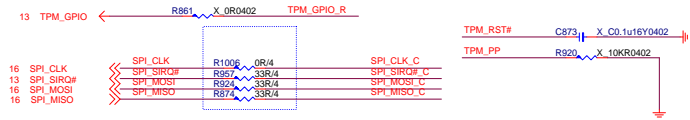
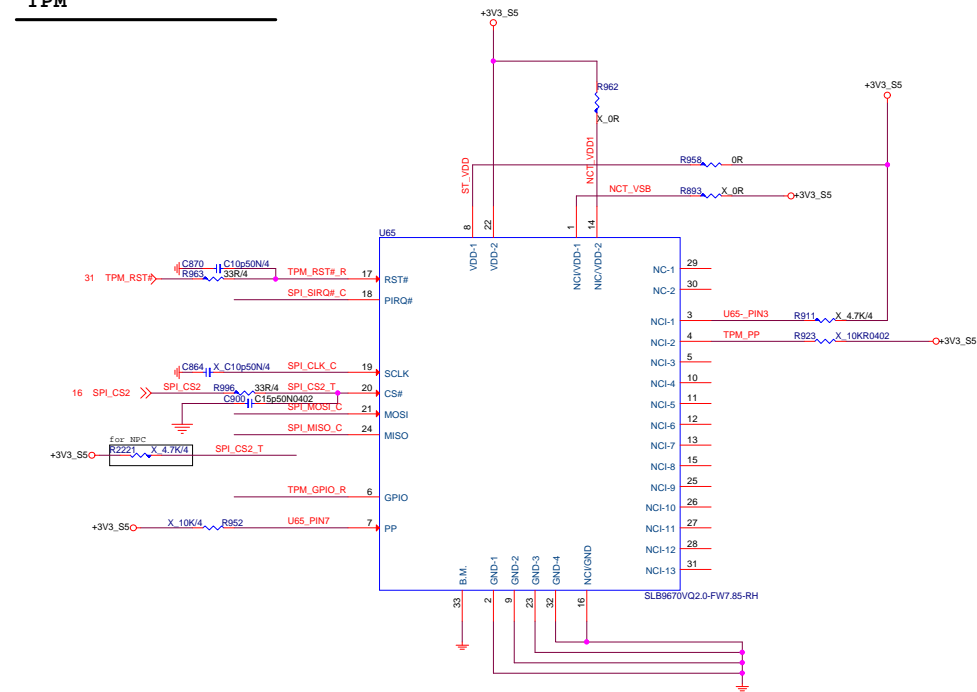
CPU\_TCK R563 0/4 PCH\_JTAGX >>> PCH\_JTAGX 14  
 CPU\_TDI R505 0/4 PCH\_JTAGTDI >>> PCH\_JTAGTDI 14  
 CPU\_TMS R506 0/4 PCH\_JTAGTMS >>> PCH\_JTAGTMS 14  
 CPU\_TDO R498 0/4 PCH\_JTAGTDO >>> PCH\_JTAGTDO 14  
 XDP\_CPU\_PRDY# R554 0/4 XDP\_PCH\_PRDY\_N >>> XDP\_PCH\_PRDY\_N 15  
 XDP\_CPU\_PREQ# R553 0/4 XDP\_PCH\_PREQ\_N >>> XDP\_PCH\_PREQ\_N 15

## USB power discharge circuit

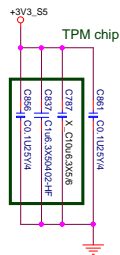
www.teknisi-indonesia.com



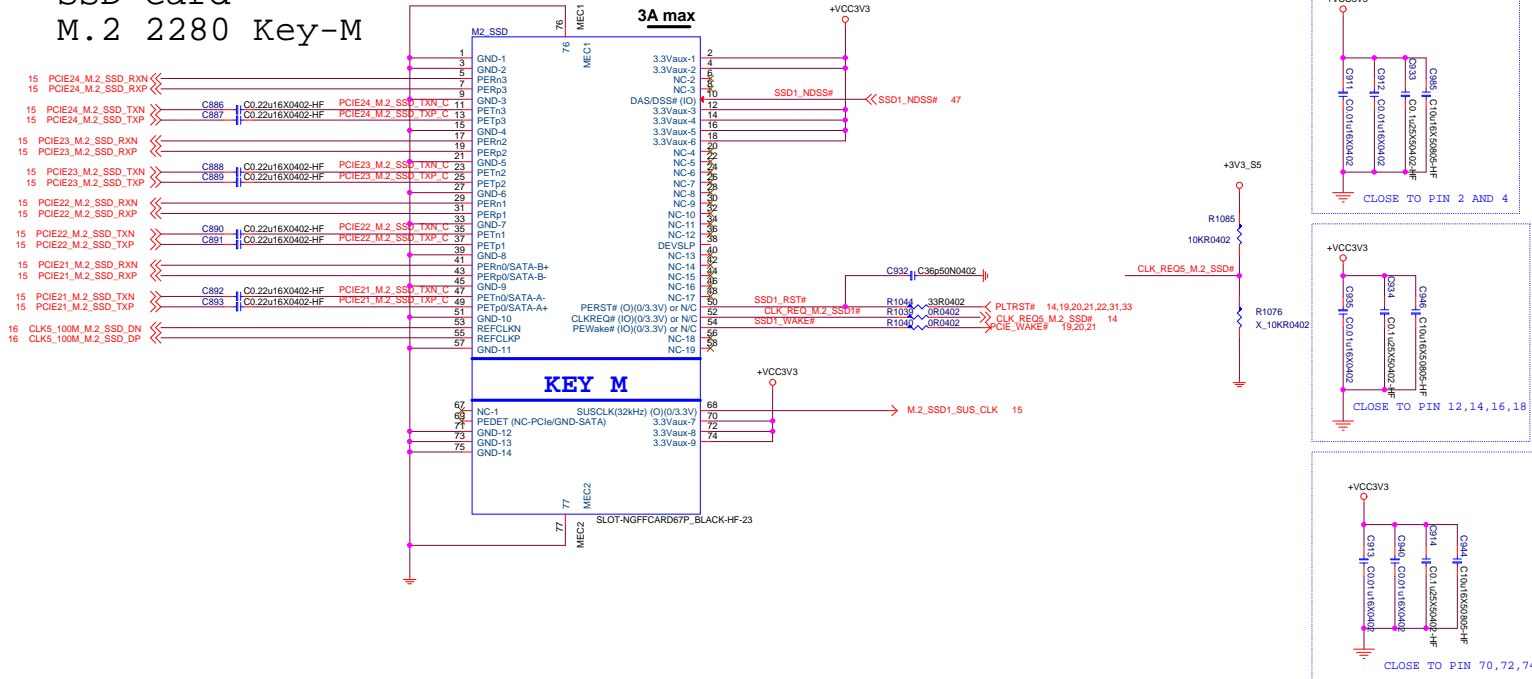
# TPM



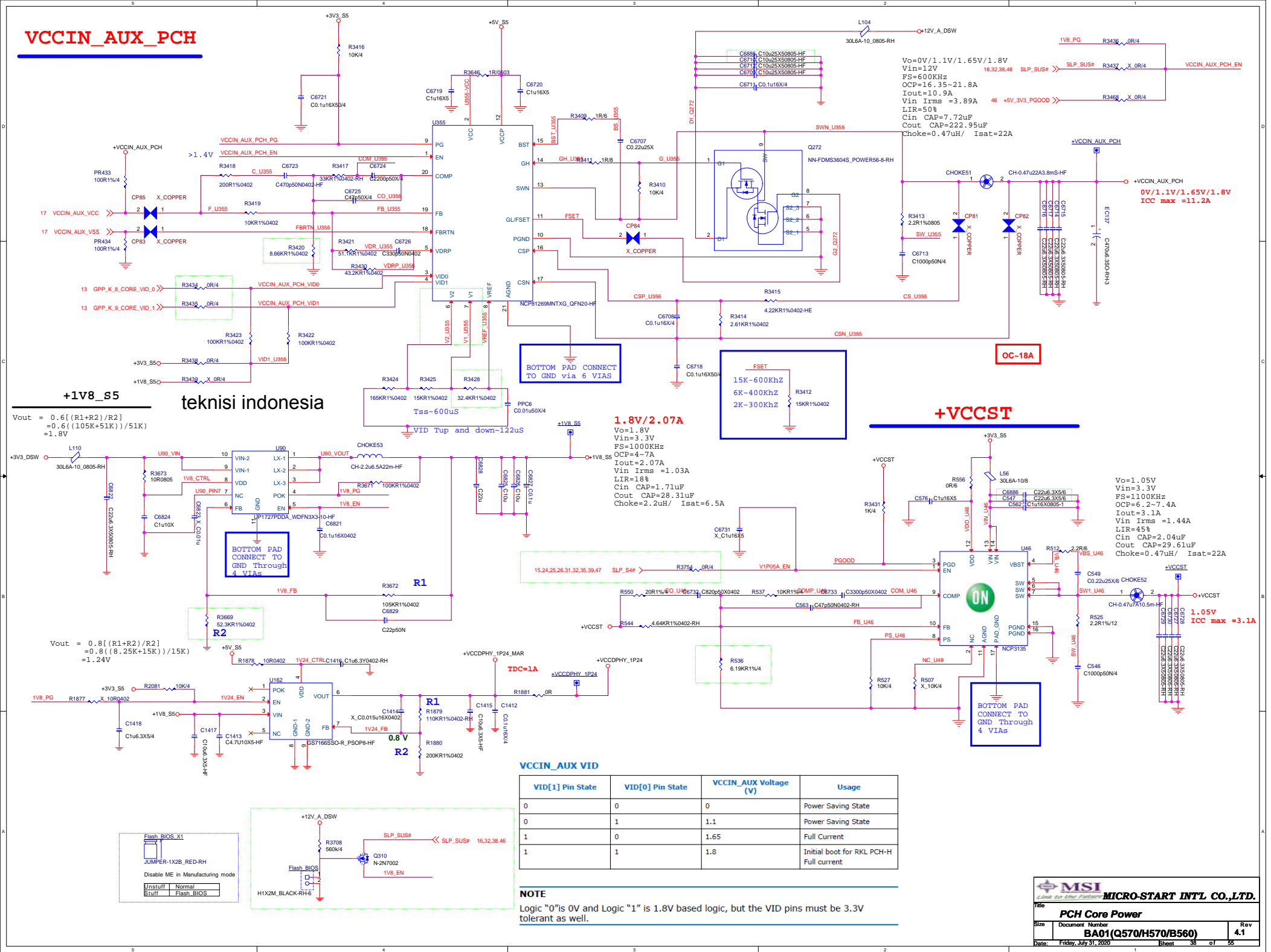
	R893	R911	R923	R920	R952	R958	R962	R861
ST----ST33HTPH2E32AHB4 (SPI)	X	X	X	X	X	X	X	X
NPC----NPCT750 SPI )	V	X	X	X	X	V	V	X
Infineon SLB 9670VQ2.0 (SPI)	X	X	X	X	X	V	X	X
NationZ Z32H330TC FW 7.51 (SPI)	V	X	X	X	X	V	V	X



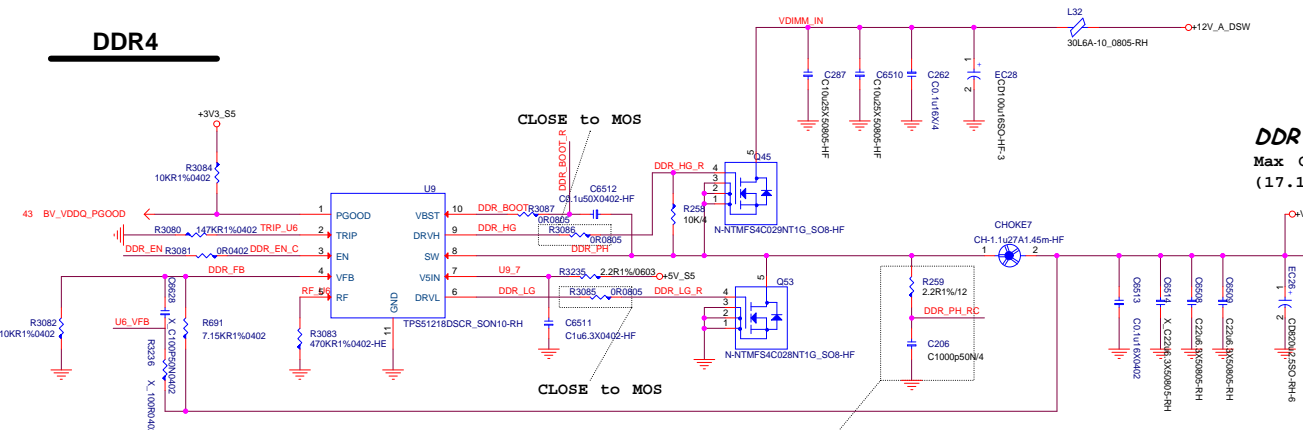
# SSD Card M.2 2280 Key-M



# VCCIN\_AUX\_PCH



## DDR4

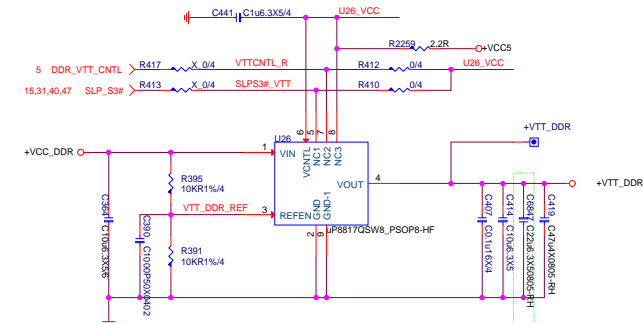


DDR  
Max Current  
(17.113A)

Vo=1.2V  
Vin=12V  
FS=300KHz  
OCP=25.67~34.23A  
Iout=17.113A  
Vrms Irms =5.13A  
LIR=19%  
Cin CAP=17.113uF  
Cout CAP=1467.51uF  
Choke=1.1uH/ Isat=27A

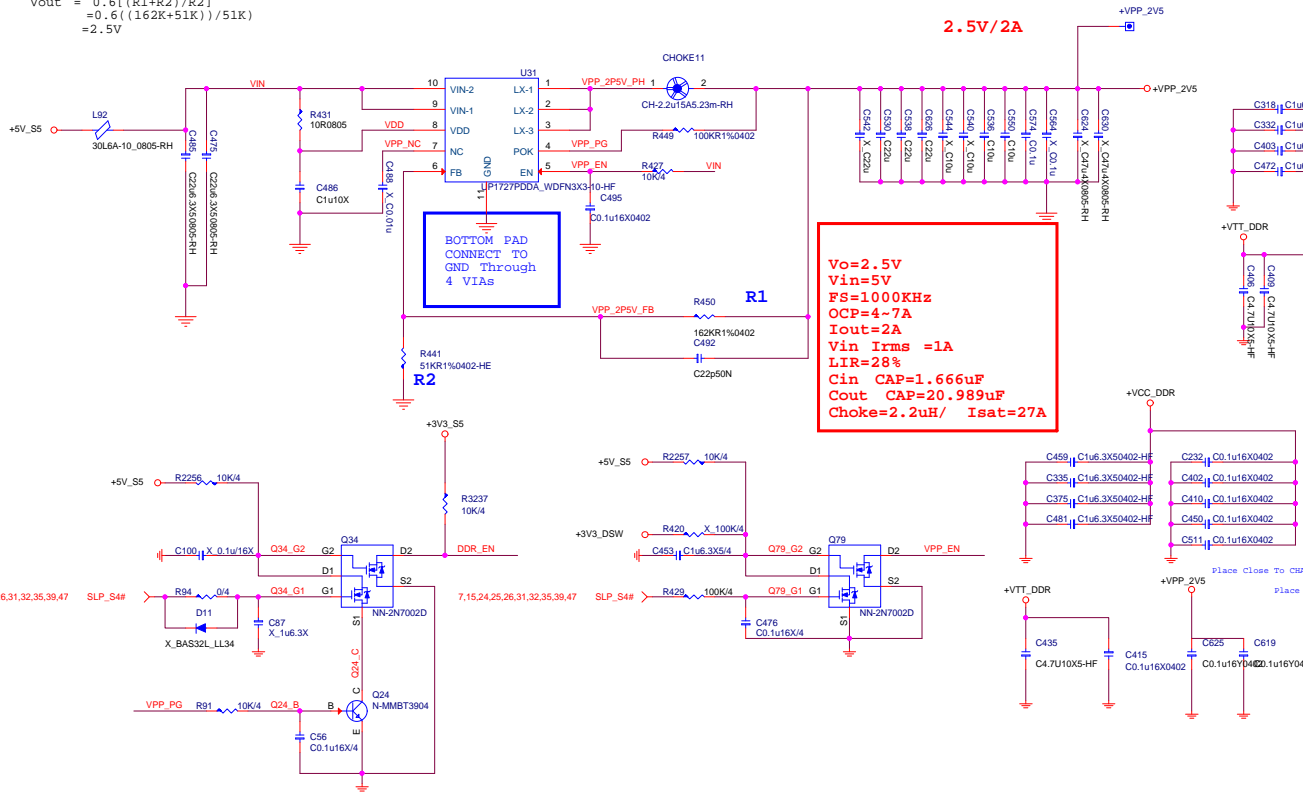
### DDR4 Termination Power

**0.6V - 1.1A - 0.825W**



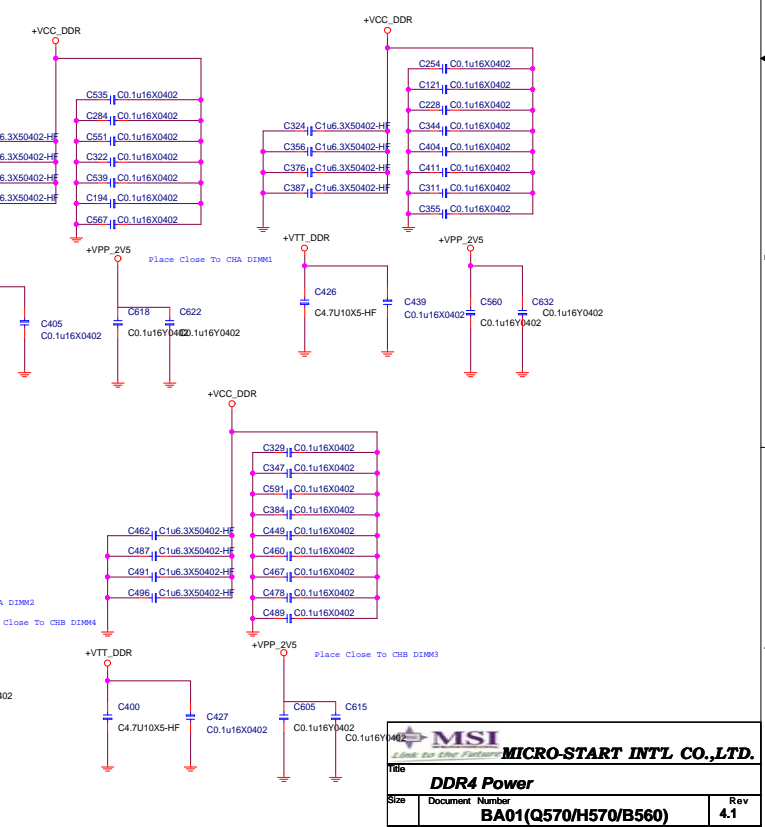
VPP\_2.5V

$$\begin{aligned} V_{out} &= 0.6[(R_1+R_2)/R_2] \\ &= 0.6((162K+51K))/51K) \\ &= 2.5V \end{aligned}$$



2.5V/2A

Vo=2.5V  
Vin=5V  
FS=1000KHz  
OCP=4~7A  
Iout=2A  
Vin Irms =1A  
LIR=28%  
Cin CAP=1.666uF  
Cout CAP=20.989uF  
Choke=2.2uH/ Isat=27A

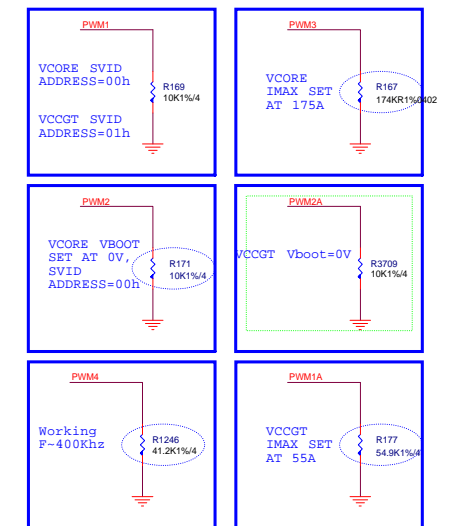
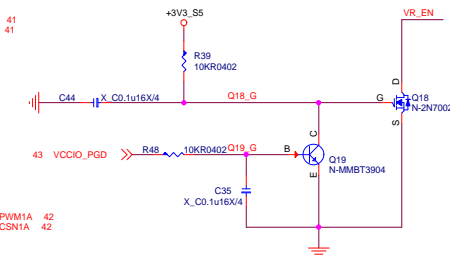
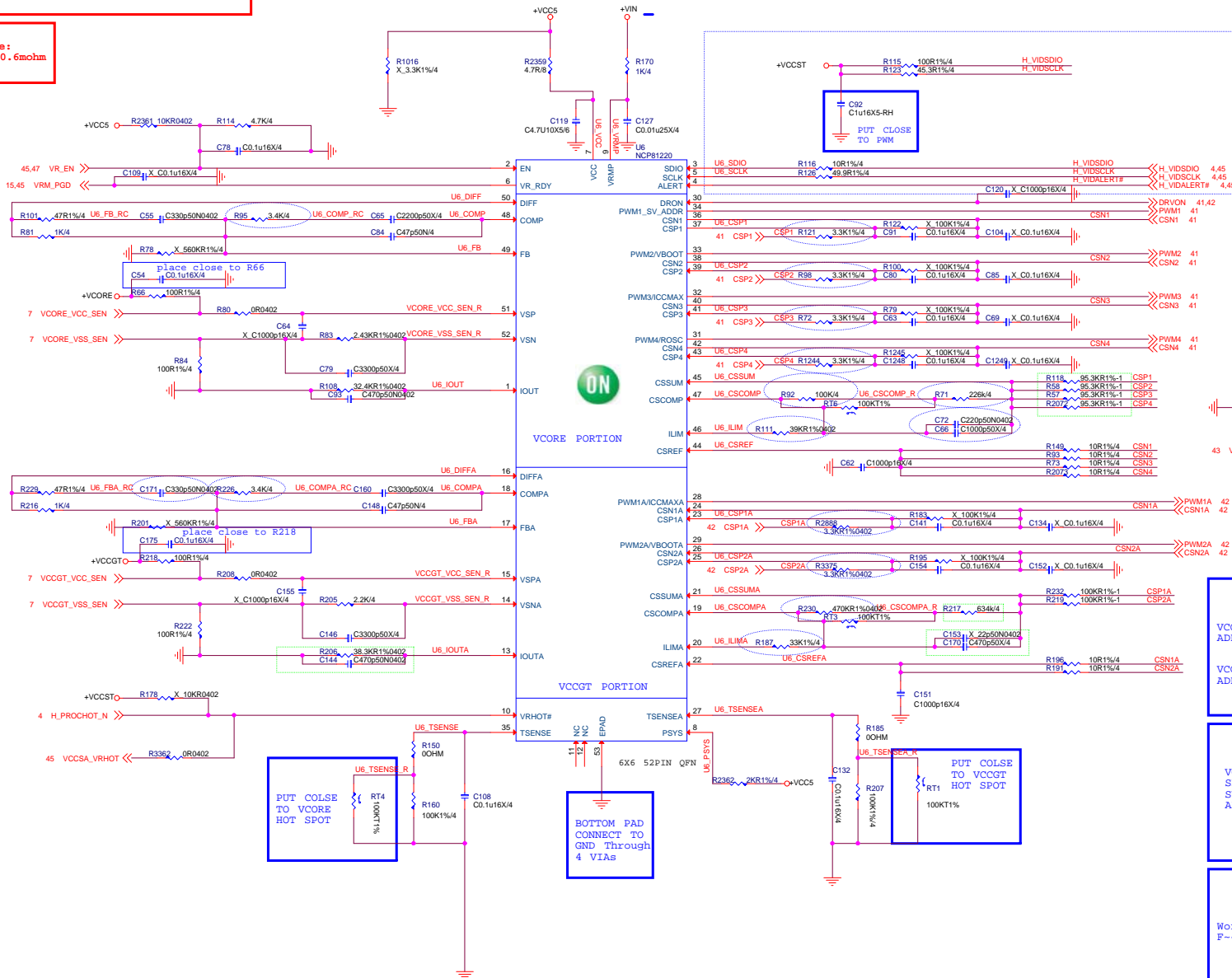




Intel RKL-S 6C\_65W - 4+2 PHASE

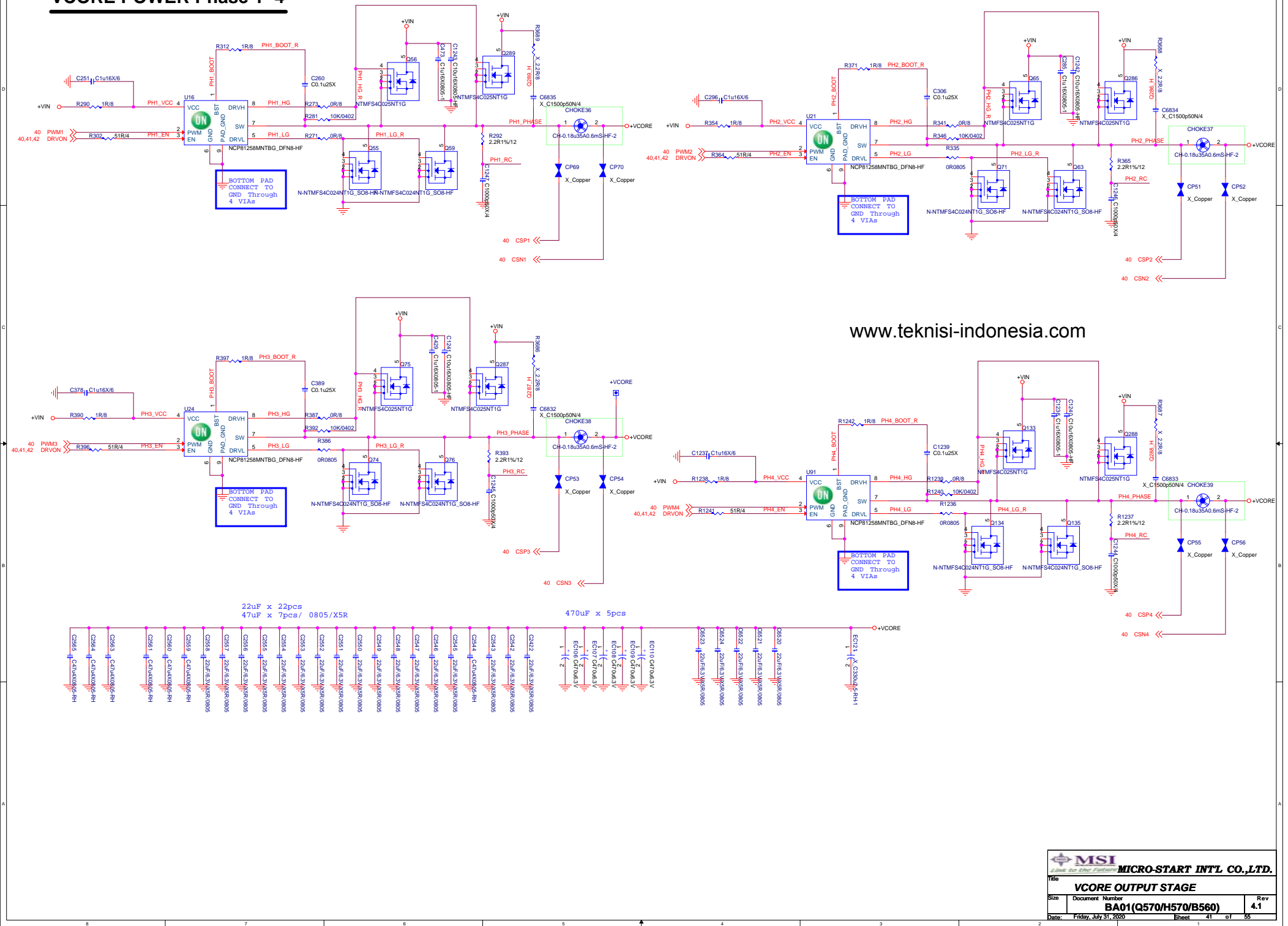
### Power Sequence

The diagram illustrates the power sequence for the NV-2N7002D MOSFET. The gate (G2) is driven by a 3V3\_S5 supply through a 10K resistor (R11). The gate is also connected to a 10nF capacitor (C3) and a 100pF capacitor (C0, 1u16X/4). The drain (D2) is connected to the VR\_EN signal. The source (S2) is connected to ground. The MOSFET is labeled NV-2N7002D. The gate is also labeled G1 and G2, and the drain is labeled D1 and D2. The source is labeled S1 and S2. The signal lines are labeled 15.31,39,47 SLP\_S3#.

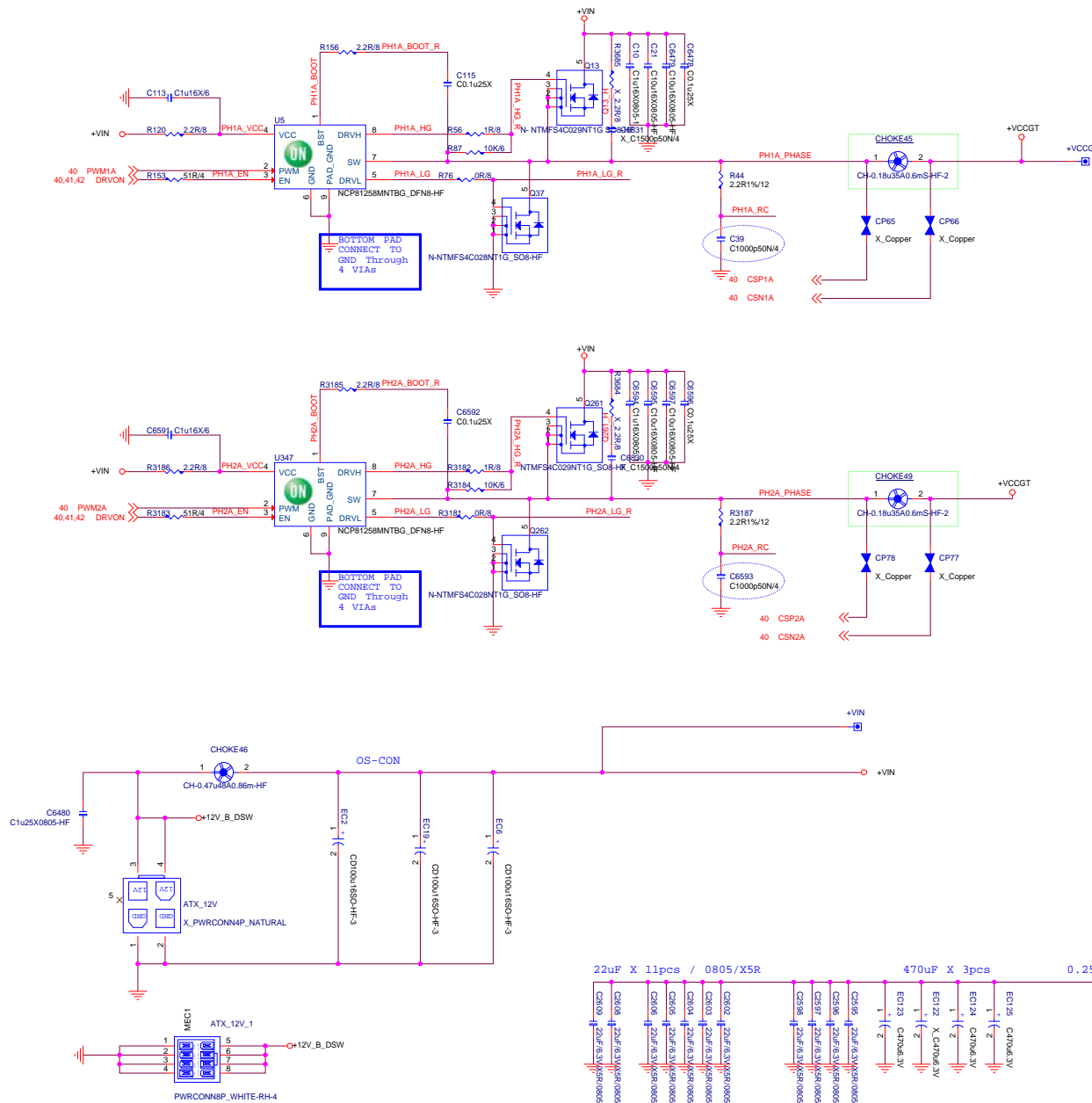




# VCORE POWER Phase 1~4

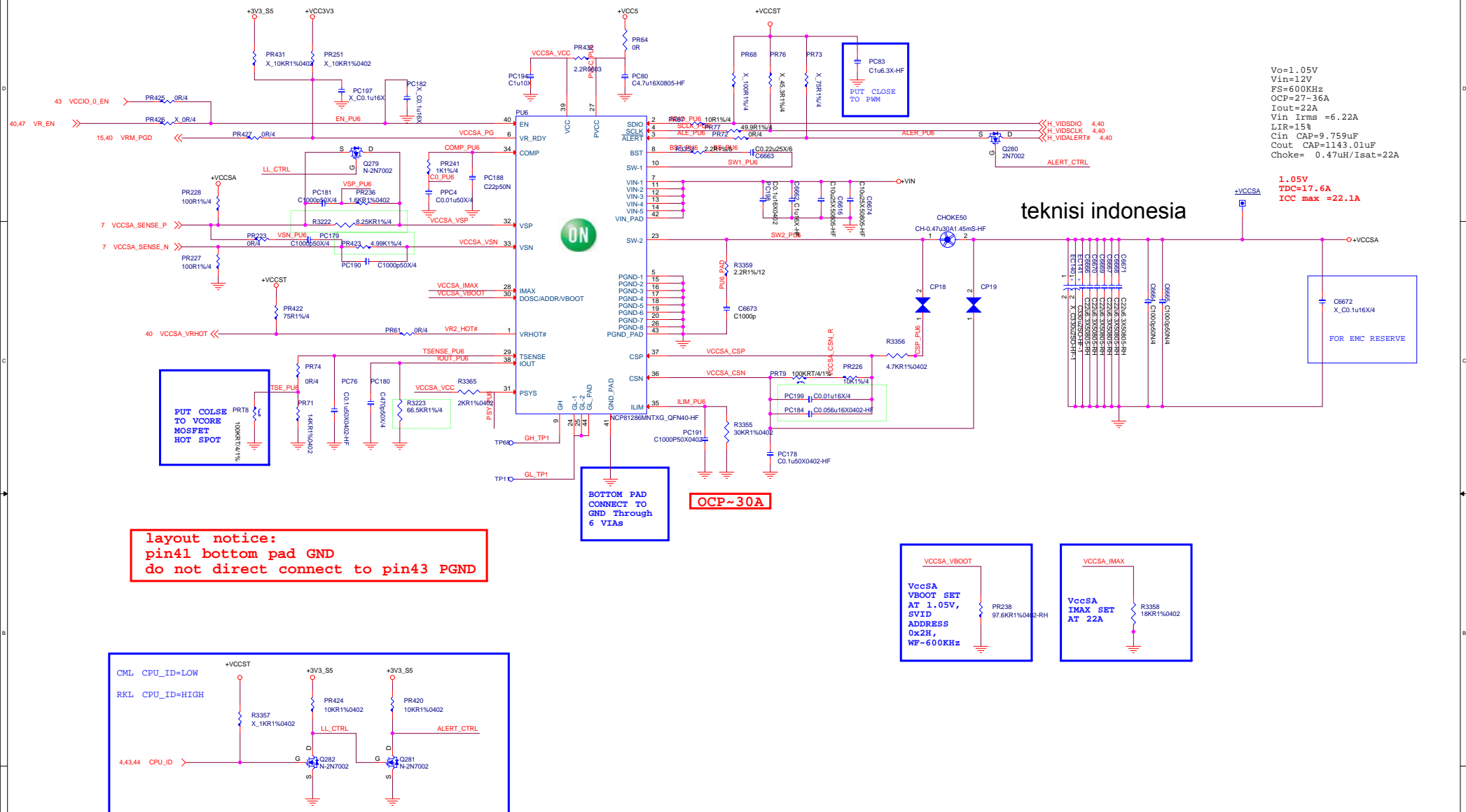


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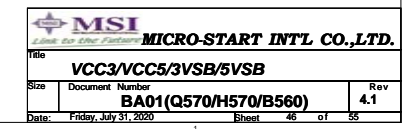




**VCC3&VCC5 Power**

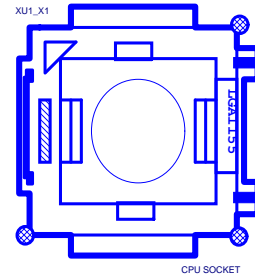
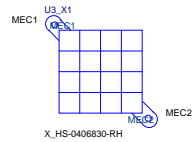
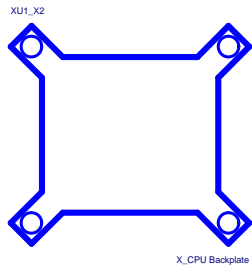
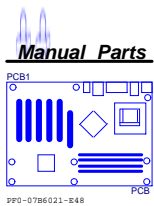
Use for Rear I

Vo=5V  
Vin=12V  
FS=300KHz  
OCP=30~40A  
Iout=20A  
Vin Irms =9.86A  
LIR=22%  
Cin CAP=54.01uF  
Cout CAP=989.66uF  
Choke=2.2uH/Isat=44A





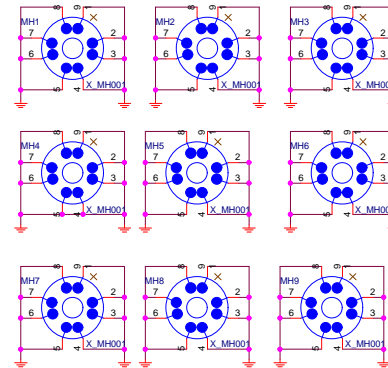
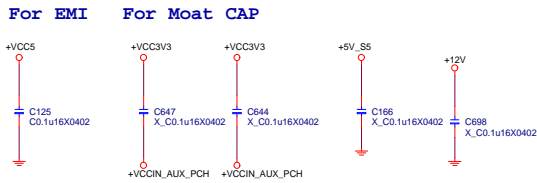




USB\_LAN5 Q570LC 6KV  
with surge single LED +USB3.0 X2 connector: N58-30F0151-F02  
USB\_LAN2 Q570LI  
without surge +USB3.0 X2 connector: N58-32F0531-S42

USB\_LAN6  
without surge +USB2.0 X2 connector: N58-23F0131-F02

USB\_LAN3 Consumer B360  
N58-21F0021-U30  
N58-21F0031-S42  
N58-21F0041-F02  
with surge single LED +USB2.0 X2 connector: N58-21F0041-F02

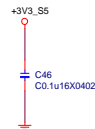


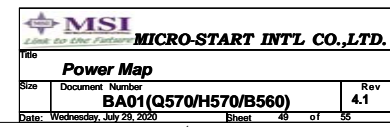
### Optics Orientation Holes

#### Optical Fiducial Marks-120

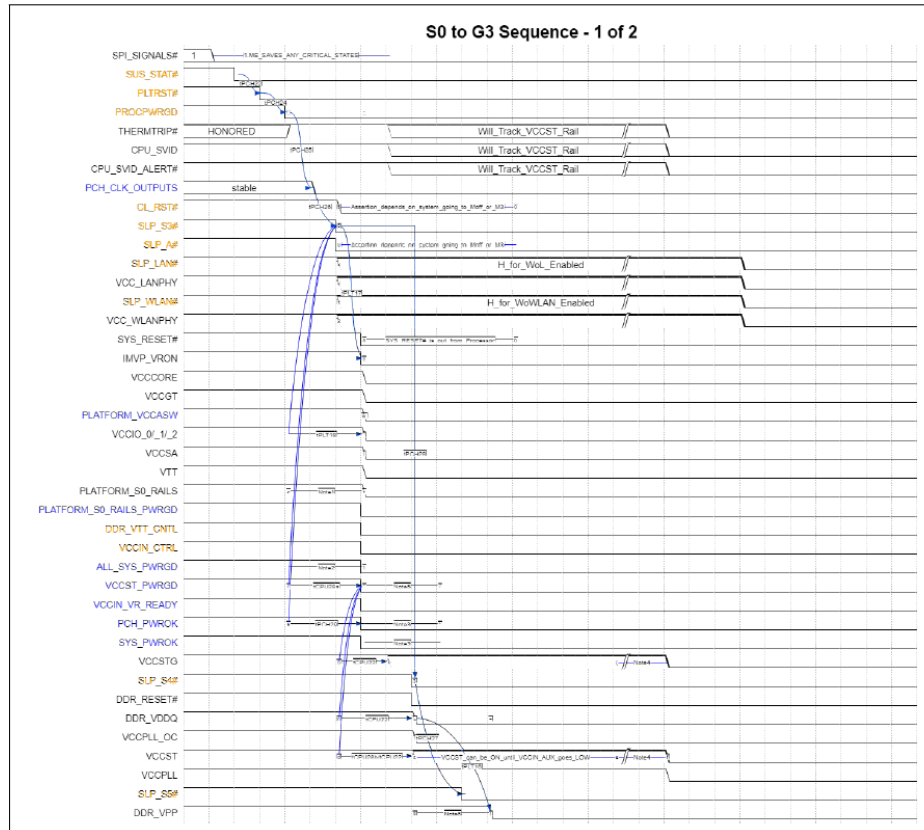


### PCH Chipset

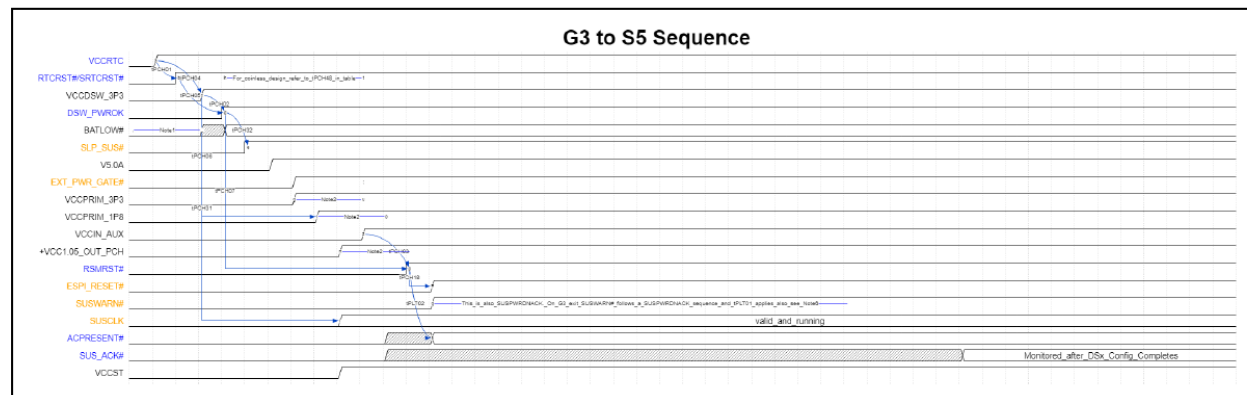




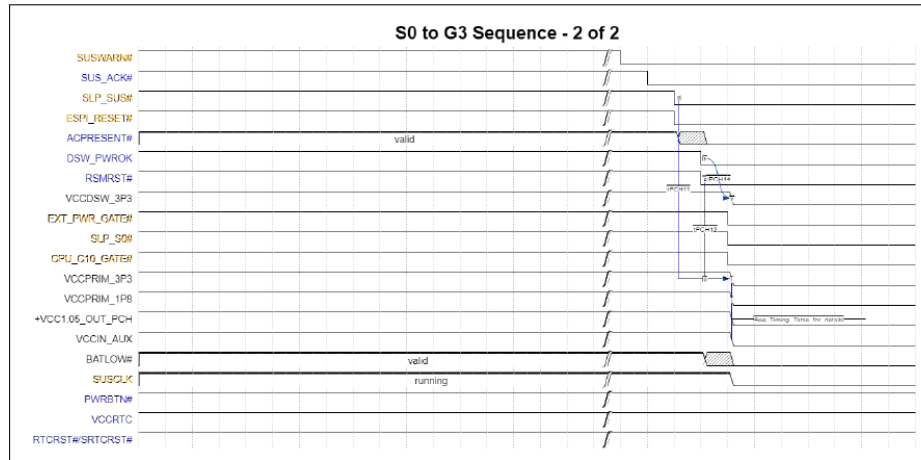
## Timing Diagram for S0/M0 to G3 [Deep Sx Platform]



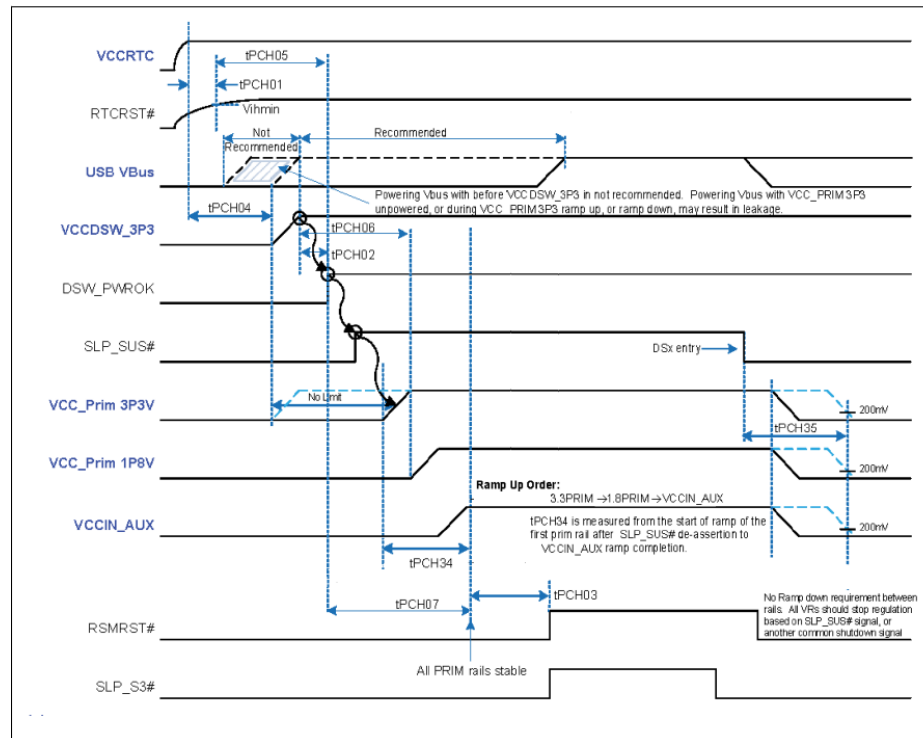
## Timing Diagram for G3 to S0 [Deep Sx Platform]

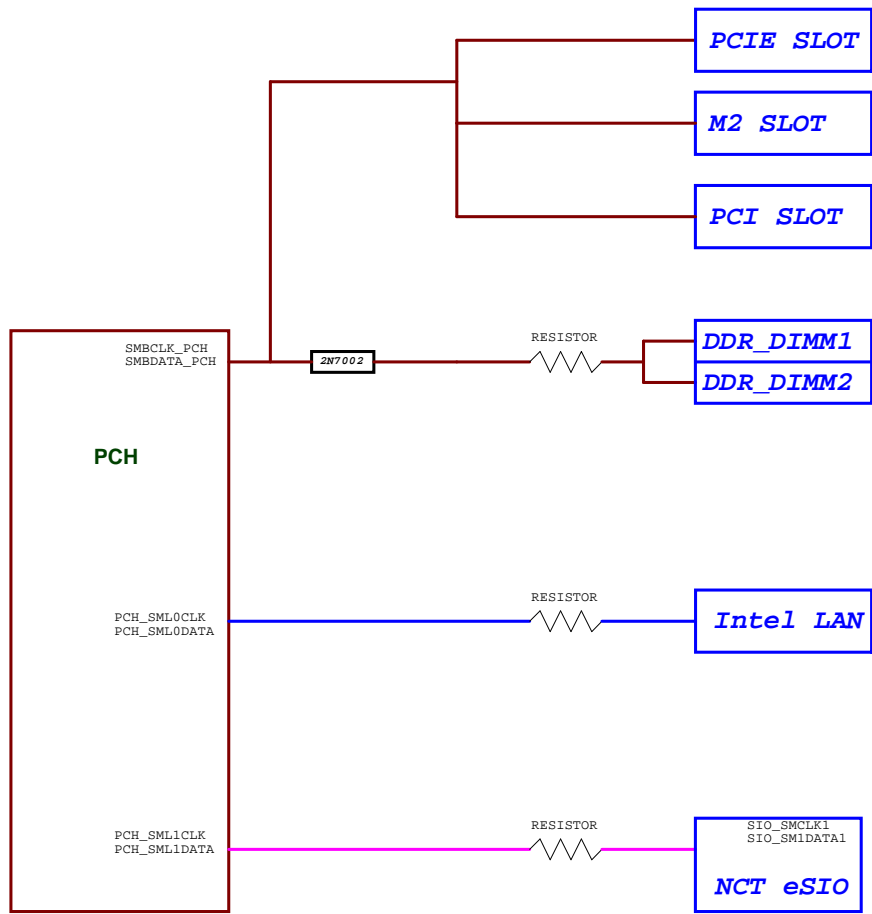


## Timing Diagram for S0/M0 to G3 [ Deep Sx Platform]

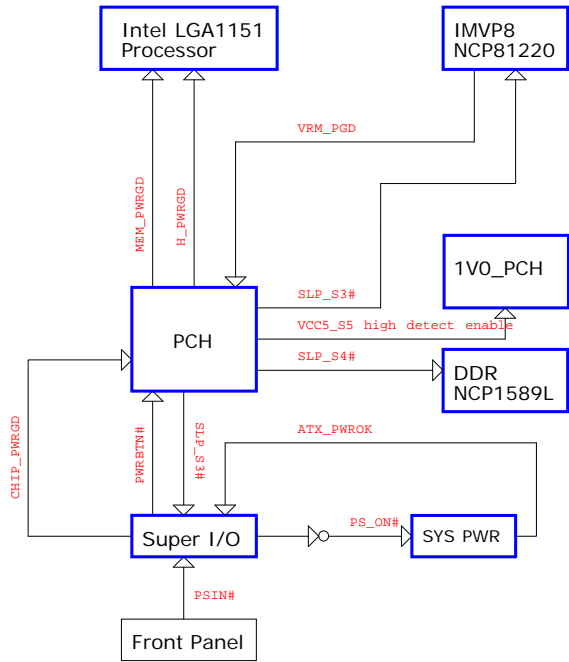


## Rail-to-Rail Sequencing Requirement for Deep Sx Configured System

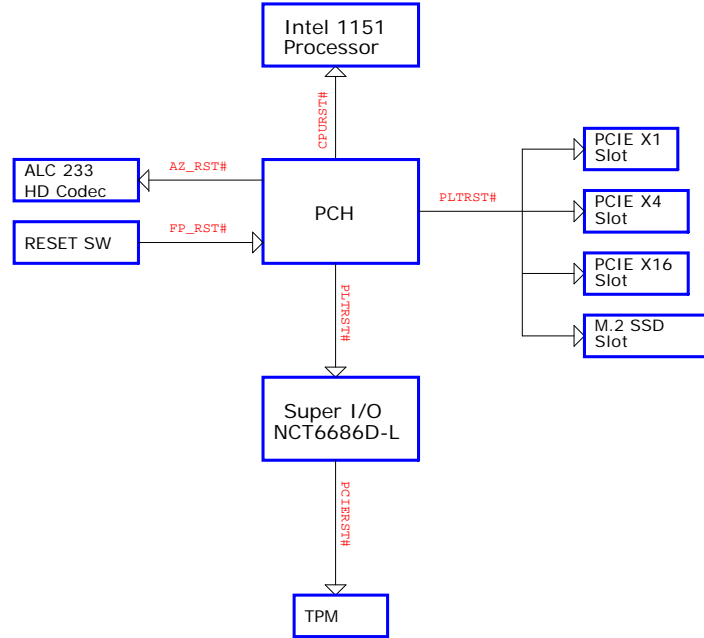




## PWROK MAP



## RESET MAP



Project	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Flexible	USB31#1	USB31#2	USB31#3	USB31#4	USB31#5	USB31#6	USB31#7	USB31#8	USB31#9	USB31#10	PCIe#5	PCIe#6	PCIe#7	PCIe#8	PCIe#9	PCIe#10	PCIe#11	PCIe#12	SATA	SATA	SATA	PCIe#17	PCIe#18	PCIe#19	PCIe#20	PCIe#21	PCIe#22	PCIe#23	PCIe#24	
TCM M80t's ROW Gen2(Q570)	Front USB3.1-2*2 Down Gen1	Front USB3.1-2*2 Up Gen1	Front USB3.1-1*2 Down Gen2	Front USB3.1-1*2 Up Gen2	Front USB3.1-type-C Gen1	Front USB3.1-type-C Gen1	Rear RJ45+USB3.1*2 down Gen1	Rear RJ45+USB3.1*2 up Gen1	Rear USB3.1*2 Down Gen1	Rear USB3.1*2 Up Gen1	RJ45 LAN port I219-LM	M2_WIFI	N/A	PCIe X1	PCIe slot3, X4, Support M.2 SSD				SATA1	SATA2	SATA3	N/A	N/A	N/A	N/A	N/A	N/A	N/A	M.2 SSD_1	
M740t/s/E98(B560)	Front USB3.1-2*2 Down Gen1	Front USB3.1-2*2 Up Gen1	Front USB3.1-1*2 Down Gen2	Front USB3.1-1*2 Up Gen2	Front USB3.1-type-A Down Gen1	Front USB3.1-type-A Up Gen1	Rear RJ45+USB2.0*2 down Gen1	Rear RJ45+USB2.0*2 up Gen1	Rear USB2.0*2 Down	Rear USB2.0*2 Up	RJ45 LAN port RTL8111K	M2_WIFI	N/A	PCIe X1	PCIe slot3, X1					SATA1	SATA2	SATA3	N/A	N/A	N/A	N/A	N/A	N/A	M.2 SSD_1	
M940t/s PRC/ M640 QT(Q570)	Front USB3.1-2*2 Down Gen1	Front USB3.1-2*2 Up Gen1	Front USB3.1-1*2 Down Gen2	Front USB3.1-1*2 Up Gen2	Front USB3.1-type-C Gen1	Front USB3.1-type-C Gen1	Rear RJ45+USB3.1*2 down Gen1	Rear RJ45+USB3.1*2 up Gen1	Rear USB3.1*2 Down Gen1	Rear USB3.1*2 Up Gen1	RJ45 LAN port I219-LM	M2_WIFI	PCI Bridge	PCIe X1	PCIe slot3, X4, Support M.2 SSD				SATA1	SATA2	SATA3	SATA4	N/A	N/A	N/A	N/A	N/A	M.2 SSD_1		
NEC ME(Q570)	Front USB3.1-2*2 Down Gen1	Front USB3.1-2*2 Up Gen1	Front USB3.1-1*2 Down Gen2	Front USB3.1-1*2 Up Gen2	Front USB3.1-type-C Gen1	Front USB3.1-type-C Gen1	Rear RJ45+USB3.1*2 down Gen1	Rear RJ45+USB3.1*2 up Gen1	Rear USB3.1*2 Down Gen1	Rear USB3.1*2 Up Gen1	RJ45 LAN port I219-LM	M2_WIFI	N/A	PCIe X1	PCIe slot3, X4, Support M.2 SSD				SATA1	SATA2	SATA3	N/A	N/A	N/A	N/A	N/A	N/A	M.2 SSD_1		
TC M747H(H570)	Front USB3.1-2*2 Down Gen1	Front USB3.1-2*2 Up Gen1	Front USB3.1-1*2 Down Gen2	Front USB3.1-1*2 Up Gen2	Front USB3.1-type-C Gen1	Front USB3.1-type-C Gen1	Rear RJ45+USB3.1*2 down Gen1	Rear RJ45+USB3.1*2 up Gen1	Rear USB2.0*2 Down	Rear USB2.0*2 Up	RJ45 LAN port RTL8111K	M2_WIFI	PCI Bridge	PCIe X1	PCIe slot3, X4, Support M.2 SSD				SATA1	SATA2	SATA3	SATA4	N/A	N/A	N/A	N/A	N/A	M.2 SSD_1		
Think ROW M70s/M70t Gen2(B560)	Front USB3.1-2*2 Down Gen1	Front USB3.1-2*2 Up Gen1	Front USB3.1-1*2 Down Gen2	Front USB3.1-1*2 Up Gen2	Front USB3.1-type-C Gen1	Front USB3.1-type-C Gen1	Rear RJ45+USB2.0*2 down Gen1	Rear RJ45+USB2.0*2 up Gen1	Rear USB2.0*2 Down	Rear USB2.0*2 Up	RJ45 LAN port I219-V	M2_WIFI	N/A	N/A	PCIe slot3, X1					SATA1	SATA2	SATA3	N/A	N/A	N/A	N/A	N/A	N/A	M.2 SSD_1	
NEC MB/LV(B560)	Front USB3.1-2*2 Down Gen1	Front USB3.1-2*2 Up Gen1	Front USB3.1-1*2 Down Gen2	Front USB3.1-1*2 Up Gen2	Front USB3.1-type-C Gen1	Front USB3.1-type-C Gen1	Rear RJ45+USB2.0*2 down Gen1	Rear RJ45+USB2.0*2 up Gen1	Rear USB2.0*2 Down	Rear USB2.0*2 Up	RJ45 LAN port I219-V	M2_WIFI	N/A	PCIe X1	PCIe slot3, X1					SATA1	SATA2	SATA3	N/A	N/A	N/A	N/A	N/A	N/A	M.2 SSD_1	
NEC ML(B560)	Front USB3.1-2*2 Down Gen1	Front USB3.1-2*2 Up Gen1	Front USB3.1-1*2 Down Gen2	Front USB3.1-1*2 Up Gen2	Front USB3.1-type-C Gen1	Front USB3.1-type-C Gen1	Rear RJ45+USB2.0*2 down Gen1	Rear RJ45+USB2.0*2 up Gen1	Rear USB2.0*2 Down	Rear USB2.0*2 Up	RJ45 LAN port I219-V	M2_WIFI	N/A	PCIe X1	PCIe slot3, X1					SATA1	SATA2	SATA3	N/A	N/A	N/A	N/A	N/A	N/A	M.2 SSD_1	
M/B 445 (B560)	Front USB3.1-2*2 Down Gen1	Front USB3.1-2*2 Up Gen1	Front USB3.1-1*2 Down Gen2	Front USB3.1-1*2 Up Gen2	Front USB3.1-type-A Down Gen1	Front USB3.1-type-A Up Gen1	Rear RJ45+USB2.0*2 down Gen1	Rear RJ45+USB2.0*2 up Gen1	Rear USB2.0*2 Down	Rear USB2.0*2 Up	RJ45 LAN port RTL8111K	M2_WIFI	PCI Bridge	PCIe X1	PCIe slot3, X1					SATA1	SATA2	SATA3	N/A	N/A	N/A	N/A	N/A	N/A	M.2 SSD_1	

2				3				2			
Signal Name		Power Well	In/Out	ATX Q570 Usage		Signal Name		Power Well	In/Out	ATX Q570 Usage	
GPP A0	GPP A0/ESPI IO0	SB1V8	NATIVE	ESPI IO0	GPP E0	GPP E0/SATAxPCIE0/SATAGP0	SB3V	OUT HIGH	N.C	GPP I11	GPP I11/USB OC4#/I2C4 SDA
GPP A1	GPP A1/ESPI IO1	SB1V8	NATIVE	ESPI IO1	GPP E1	GPP E1/SATAxPCIE1/SATAGP1	SB3V	OUT HIGH	N.C	GPP I12	GPP I12/USB OC5#/I2C4 SCL
GPP A2	GPP A2/ESPI IO2/SUSWARN#/SUSPWRDNACK	SB1V8	NATIVE	ESPI IO2	GPP E2	GPP E2/SATAxPCIE2/SATAGP2	SB3V	OUT HIGH	N.C	GPP I13	GPP I13/USB OC6#/I2C5 SDA
GPP A3	GPP A3/ESPI IO3/SUSACK#	SB1V8	NATIVE	ESPI IO3	GPP E3	GPP E3/CPU GP0	SB3V	OUT HIGH	N.C	GPP I14	GPP I14/USB OC7#/I2C5 SCL
GPP A4	GPP A4/ESPI CS0#	SB1V8	NATIVE	ESPI CS0#	GPP E4	GPP E4/SATA DEVSLP0	SB3V	OUT HIGH	N.C	GPP J0	GPP J0/CNV PA BLANKING
GPP A5	GPP A5/ESPI CLK	SB1V8	NATIVE	ESPI CLK R	GPP E5	GPP E5/SATA DEVSLP1	SB3V	OUT HIGH	N.C	GPP J1	GPP J1/CPU C10 GATE#
GPP A6	GPP A6/ESPI RESET#	SB1V8	NATIVE	ESPI RESET# R	GPP E6	GPP E6/SATA DEVSLP2	SB3V	OUT HIGH	N.C	GPP J2	GPP J2/CNV BRI DT/UART0 RTS#
GPP A7	GPP A7/ESPI CS1#	SB1V8	OUT HIGH	N.C	GPP E7	GPP E7/CPU GP1	SB3V	IN	SKTOCC# C	GPP J3	GPP J3/CNV BRI RSP/UART0 RxD
GPP A8	GPP A8/ESPI CS2#	SB1V8	OUT HIGH	N.C	GPP E8	GPP E8/SATALED#/SP11 CS1#	SB3V	NATIVE	SATA LED#	GPP J4	GPP J4/CNV RGI DT/UART0 TXD
GPP A9	GPP A9/ESPI CS3#	SB1V8	OUT HIGH	N.C	GPP E9	GPP E9/USB OC0#	SB3V	NATIVE	USB OC#0	GPP J6	GPP J6/CNV RGI RSP/UART0 CTS#
GPP A10	GPP A10/ESPI ALERT0#	SB1V8	NATIVE	ESPI ALERT0#	GPP E10	GPP E10/USB OC1#	SB3V	NATIVE	USB OC#1	GPP J7	GPP J7
GPP A11	GPP A11/ESPI ALERT1#	SB1V8	OUT HIGH	N.C	GPP E11	GPP E11/USB OC2#	SB3V	NATIVE	USB OC#2	GPP J8	GPP J8
GPP A12	GPP A12/ESPI ALERT2#	SB1V8	OUT HIGH	N.C	GPP E12	GPP E12/USB OC3#	SB3V	NATIVE	USB OC#3	GPP J9	GPP J9
GPP A13	GPP A13/ESPI ALERT3#	SB1V8	OUT HIGH	N.C	GPP F0	GPP F0/SATAxPCIE3/SATAGP3	SB3V	IN	PCH GPIO F0	GPP J0	GPP J0/GSxDOUT
GPP A14	GPP A14/MGCLKOUT0	SB1V8	OUT HIGH	N.C	GPP F1	GPP F1/SATAxPCIE4/SATAGP4	SB3V	OUT HIGH	N.C	GPP K1	GPP K1/GSxSLOAD
GPP B0	GPP B0/GSPI0 CS1#/MGCLKOUT1	SB3V	OUT HIGH	N.C	GPP F2	GPP F2/SATAxPCIE5/SATAGP5	SB3V	OUT HIGH	N.C	GPP K2	GPP K2/GSxDIN
GPP B1	GPP B1/GSPI1 CS1#/TIME SYNC1	SB3V	OUT HIGH	N.C	GPP F3	GPP F3/SATAxPCIE6/SATAGP6	SB3V	OUT HIGH	N.C	GPP K3	GPP K3/GSxSRESET#
GPP B2	GPP B2/VALERIT#	SB3V	IN	CNV UART WAKE#	GPP F4	GPP F4/SATAxPCIE7/SATAGP7	SB3V	OUT HIGH	N.C	GPP K4	GPP K4/GSxSCLK
GPP B3	GPP B3/CPU GP2	SB3V	OUT HIGH	WIRELESS EN2	GPP F5	GPP F5/SATA DEVSLP3	SB3V	IN	SPI SI/Q#	GPP K5	GPP K5/ADR COMPLETE
GPP B4	GPP B4/CPU GP3	SB3V	OUT HIGH	N.C	GPP F6	GPP F6/SATA DEVSLP4	SB3V	NATIVE	PCH GPIO F6	GPP K6	GPP K6/DDSP HPDA/DISP MISCA
GPP B5	GPP B5/SRCLCLKREQ0#	SB3V	NATIVE	CLK REQ0 PCIE16#	GPP F7	GPP F7/SATA DEVSLP5	SB3V	OUT HIGH	N.C	GPP K7	GPP K7/DDSP HPDB/DISP MISCB
GPP B6	GPP B6/SRCLCLKREQ1#	SB3V	NATIVE	CLK REQ1 PCIE1#	GPP F8	GPP F8/SATA DEVSLP6	SB3V	OUT HIGH	N.C	GPP K8	GPP K8/CORE VID0
GPP B7	GPP B7/SRCLCLKREQ2#	SB3V	NATIVE	CLK REQ2 PCIE4#	GPP F9	GPP F9/SATA DEVSLP7	SB3V	OUT HIGH	N.C	GPP K9	GPP K9/CORE VID1
GPP B8	GPP B8/SRCLCLKREQ3#	SB3V	NATIVE	CLK REQ3 M.2 WLAN#	GPP F10	GPP F10/SATA S/CLOCK	SB3V	OUT HIGH	N.C	GPP K10	GPP K10/DDSP HPDC/DISP MISCC
GPP B9	GPP B9/SRCLCLKREQ4#	SB3V	OUT HIGH	N.C	GPP F11	GPP F11/SATA S/LOAD	SB3V	OUT HIGH	N.C	GPP K11	GPP K11
GPP B10	GPP B10/SRCLCLKREQ5#	SB3V	NATIVE	CLK REQ5 M.2 SSD#	GPP F12	GPP F12/SATA SDATAOUT1	SB3V	OUT HIGH	N.C	GP00	GP00/BATLOW#
GPP B11	GPP B11/1/2S MCLK	SB3V	OUT HIGH	N.C	GPP F13	GPP F13/SATA SDATAOUT0	SB3V	OUT HIGH	N.C	GP01	GP01/ACPRESENT
GPP B12	GPP B12/SLP S0#	SB3V	NATIVE	SLP S0#	GPP F14	GPP F14/PS ON#	SB3V	NATIVE	PS ON B	GP02	GP02/LAN WAKE#
GPP B13	GPP B13/PLTRST#	SB3V	NATIVE	PLTRST#	GPP F15	GPP F15/M2 SKT2 CFG0	SB3V	NATIVE	TPM GPIO	GP03	GP03/PWRBTN#
GPP B14	GPP B14/SPKR	SB3V	NATIVE	SPKR	GPP F16	GPP F16/M2 SKT2 CFG1	SB3V	IN	POL#	GP04	GP04/SLP S3#
GPP B15	GPP B15/GSPI0 CS0#	SB3V	OUT HIGH	N.C	GPP F17	GPP F17/M2 SKT2 CFG2	SB3V	NATIVE	SIO SCI N	GP05	GP05/SLP S4#
GPP B16	GPP B16/GSPI0 CLK	SB3V	OUT HIGH	N.C	GPP F18	GPP F18/M2 SKT2 CFG3	SB3V	OUT HIGH	PCH GPIO F18	GP06	GP06/SLP A#
GPP B17	GPP B17/GSPI0 MISO	SB3V	OUT HIGH	N.C	GPP F19	GPP F19/EDP VDDEN	SB3V	OUT HIGH	N.C	GP07	GP07
GPP B18	GPP B18/GSPI0 MOSI	SB3V	NATIVE	REBOOT STRAP	GPP F20	GPP F20/EDP BKLTEN	SB3V	OUT HIGH	N.C	GP08	GP08/SUSCLK
GPP B19	GPP B19/GSPI1 CS0#	SB3V	OUT HIGH	N.C	GPP F21	GPP F21/EDP BKLTCTL	SB3V	OUT HIGH	N.C	GP09	GP09/SLP WLAN#
GPP B20	GPP B20/GSPI1 CLK	SB3V	NATIVE	SMI#	GPP F22	GPP F22/VNN CTRL	SB3V	OUT HIGH	VCCIO VID1	GPD10	GPD10/SLP S5#
GPP B21	GPP B21/GSPI1 MISO	SB3V	OUT HIGH	N.C	GPP F23	GPP F23	SB3V	OUT HIGH	VCCIO VID2	GPD11	GPD11/LANPHYC
GPP B22	GPP B22/GSPI1 MOSI	SB3V	NATIVE	BBS STRAP	GPP G0	GPP G0/DDPA CTRLCLK	SB3V	IN	CHASSIS ID1	GPD12	GPD12
GPP B23	GPP B23/SML1ALERT#/PCHHOT#	SB3V	NATIVE	SMLINK1 ALERT N	GPP G1	GPP G1/DDPA CTRLDATA	SB3V	IN	CHASSIS ID2	GPP R0	GPP R0/HDA BCLK/I2S0 SCLK/HDACPU BCLK
GPP C0	GPP C0/SMBCLK	SB3V	NATIVE	SMBCLK R	GPP G2	GPP G2/DNX FORCE RELOAD	SB3V	OUT HIGH	H PROCHOT PCH N	GPP R1	GPP R1/HDA SYNC/I2S0 SFRM
GPP C1	GPP C1/SMBDATA	SB3V	NATIVE	SMBDATA R	GPP G3	GPP G3	SB3V	OUT HIGH	N.C	GPP R2	GPP R2/HDA SDO/I2S0 TXD/HDACPU SDO
GPP C2	GPP C2/SMBALERT#	SB3V	NATIVE	TLS STRAP	GPP G4	GPP G4	SB3V	OUT HIGH	N.C	GPP R3	GPP R3/HDA SDIO/I2S0 RXD/HDACPU SDI
GPP C3	GPP C3/ISH UART0 RxD/I2C2 SDA	SB3V	OUT HIGH	N.C	GPP G5	GPP G5/SLP DRAM#	SB3V	OUT HIGH	N.C	GPP R4	GPP R4/HDA RST#
GPP C4	GPP C4/ISH UART0 TXD/I2C2 SCL	SB3V	OUT HIGH	N.C	GPP G6	GPP G6	SB3V	OUT HIGH	N.C	GPP R5	GPP R5/HDA SDI1/I2S1 RxD
GPP C5	GPP C5/SML0ALERT#	SB3V	NATIVE	ESPI STRAP	GPP G7	GPP G7	SB3V	OUT HIGH	N.C	GPP R6	GPP R6/I2S1 TXD
GPP C6	GPP C6/ISH I2C2 SDA/I2C3 SDA/SBK4/BK4	SB3V	OUT HIGH	N.C	GPP G8	GPP G8/ISH SPI CS#/DDP3 CTRLCLK/GSPI2 C	SB3V	OUT HIGH	N.C	GPP R7	GPP R7/I2S1 SFRM
GPP C7	GPP C7/ISH I2C2 SCL/I2C3 SCL	SB3V	OUT HIGH	N.C	GPP G9	GPP G9/ISH SPI CLK/DDP3 CTRLDATA/GSPI2 C	SB3V	OUT HIGH	N.C	GPP R8	GPP R8/I2S1 SCLK
GPP C8	GPP C8/UART0 RxD	SB3V	IN	CLR CMOS	GPP G10	GPP G10/ISH SPI MISO/DDP4 CTRLCLK/GSPI2 C	SB3V	OUT HIGH	N.C	GPP R9	GPP R9/PCIE LNK DOWN
GPP C9	GPP C9/UART0 TXD	SB3V	OUT HIGH	N.C	GPP G11	GPP G11/ISH SPI MOSI/DDP4 CTRLDATA/GSPI2 C	SB3V	OUT HIGH	N.C	GPP R10	GPP R10/ISH UART0 RTS#/GSPi2 CS1#
GPP C10	GPP C10/UART0 RTS#	SB3V	OUT HIGH	N.C	GPP G12	GPP G12/DDP1 CTRLCLK/TBT LSX0 TXD	SB3V	NATIVE	DP DDPC CTRLCLK	GPP R11	GPP R11/SX EXIT HOLDOFF#/ISH GP6
GPP C11	GPP C11/UART0 CTS#	SB3V	OUT HIGH	N.C	GPP G13	GPP G13/DDP1 CTRLDATA/TBT LSX0 RxD	SB3V	NATIVE	DP DDPC CTRLDATA	GPP R12	GPP R12/CLKOUT 48
GPP C12	GPP C12/UART1 RxD/ISH UART1 RxD	SB3V	OUT HIGH	N.C	GPP G14	GPP G14/DDP2 CTRLCLK/TBT LSX1 TXD	SB3V	NATIVE	DP DDPC CTRLCLK	GPP R13	GPP R13/ISH GP7
GPP C13	GPP C13/UART1 TXD/ISH UART1 TXD	SB3V	OUT HIGH	N.C	GPP G15	GPP G15/DDP2 CTRLDATA/TBT LSX1 RxD	SB3V	NATIVE	DP DDPC CTRLDATA	GPP R14	GPP R14/ISH GP0
GPP C14	GPP C14/UART1 RTS#/ISH UART1 RTS#	SB3V	OUT HIGH	N.C	GPP H0	GPP H0/SRCLCLKREQ6#	SB3V	NATIVE	CLK REQ6 LAN #	GPP R15	GPP R15/ISH GP1
GPP C15	GPP C15/UART1 CTS#/ISH UART1 CTS#	SB3V	OUT HIGH	N.C	GPP H1	GPP H1/SRCLCLKREQ7#	SB3V	OUT HIGH	N.C	GPP R16	GPP R16/ISH GP2
GPP C16	GPP C16/I2C0 SDA	SB3V	OUT HIGH	N.C	GPP H2	GPP H2/SRCLCLKREQ8#	SB3V	IN	FM CATERR N	GPP R17	GPP R17/ISH GP3
GPP C17	GPP C17/I2C0 SCL	SB3V	OUT HIGH	N.C	GPP H3	GPP H3/SRCLCLKREQ9#	SB3V	OUT HIGH	N.C	GPP R18	GPP R18/ISH GP4
GPP C18	GPP C18/I2C1 SDA	SB3V	OUT HIGH	N.C	GPP H4	GPP H4/SRCLCLKREQ10#	SB3V	OUT HIGH	N.C	GPP R19	GPP R19/ISH GP5
GPP C19	GPP C19/I2C1 SCL	SB3V	OUT HIGH	N.C	GPP H5	GPP H5/SRCLCLKREQ11#	SB3V	OUT HIGH	N.C	GPP S0	GPP S0/SNDW1 CLK
GPP C20	GPP C20/UART2 RxD	SB3V	OUT HIGH	N.C	GPP H6	GPP H6/SRCLCLKREQ12#	SB3V	IN	GPIO WLAN WAKE N	GPP S1	GPP S1/SNDW1 DATA
GPP C21	GPP C21/UART2 TXD	SB3V	OUT HIGH	N.C	GPP H7	GPP H7/SRCLCLKREQ13#	SB3V	OUT HIGH	N.C	GPP S2	GPP S2/SNDW2 CLK/DMIC CLKB0
GPP C22	GPP C22/UART2 RTS#	SB3V	OUT HIGH	N.C	GPP H8	GPP H8/SRCLCLKREQ14#	SB3V	OUT HIGH	N.C	GPP S3	GPP S3/SNDW2 CLK/DMIC CLKB1
GPP C23	GPP C23/UART2 CTS#	SB3V	OUT HIGH	N.C	GPP H9	GPP H9/SRCLCLKREQ15#	SB3V	OUT HIGH	N.C	GPP S4	GPP S4/SNDW3 CLK/DMIC CLKA1
GPP D0	GPP D0/THC0 SPI1 CS#/SBK0/BK0	SB1V8	OUT HIGH	N.C	GPP H10	GPP H10/SML2CLK	SB3V	OUT HIGH	N.C	GPP S5	GPP S5/SNDW3 DATA/DMIC DATA1
GPP D1	GPP D1/THC0 SPI1 CLK/SBK1/BK1	SB1V8	OUT HIGH	PW LED N	GPP H11	GPP H11/SML2ADATA	SB3V	OUT HIGH	WIRELESS EN		
GPP D2	GPP D2/THC0 SPI1 IO1/SBK2/BK2	SB1V8	OUT HIGH	N.C	GPP H12	GPP H12/SML2ALERT#	SB3V	NATIVE	FM ESPI FLASH MODE		
GPP D3	GPP D3/THC0 SPI1 IO0/SBK3/BK3	SB1V8	OUT HIGH	N.C	GPP H13	GPP H13/SML3CLK	SB3V	OUT HIGH	LAN PON		
GPP D4	GPP D4/SML1CLK	SB1V8	NATIVE	SML1 CLK PCH	GPP H14	GPP H14/SML3DATA	SB3V	OUT HIGH	N.C		
GPP D5	GPP D5/I2S2 SFRM/CNV RF RESET#	SB1V8	NATIVE	CNV RF RESET#	GPP H15	GPP H15/SML3ALERT#	SB3V	IN	PCH GPP H15		
GPP D6	GPP D6/I2S2 TXD/MODEM CLKREQ	SB1V8	NATIVE	CNV PCM OUT	GPP H16	GPP H16/SML4CLK	SB3V	OUT HIGH	N.C		
GPP D7	GPP D7/I2S2 RxD/THC0 SPI1 RST#	SB1V8	NATIVE	CNV PCM IN	GPP H17	GPP H17/SML4DATA	SB3V	OUT HIGH	N.C		
GPP D8	GPP D8/I2S2 SCLK/THC0 SPI1 INT#	SB1V8	NATIVE	CNV PCM CLK	GPP H18	GPP H18/SML4ALERT#	SB3V	NATIVE	PCH GPP H18		
GPP D9	GPP D9/SML0CLK	SB1V8	NATIVE	SML0 CLK PCH	GPP H19	GPP H19/ISH I2C0 SDA	SB3V	OUT HIGH	N.C		
GPP D10	GPP D10/SML0DATA	SB1V8	NATIVE	SML0 DATA PCH	GPP H20	GPP H20/ISH I2C0 SCL	SB3V	OUT HIGH	N.C		
GPP D11	GPP D11	SB1V8	IN	FUSB G1	GPP H21	GPP H21/ISH I2C1 SDA	SB3V	IN	COM DET#		
GPP D12	GPP D12/ISH UART0 CTS#	SB1V8	IN	FUSB G2	GPP H22	GPP H22/ISH I2C1 SCL	SB3V	OUT HIGH	N.C		
GPP D13	GPP D13/THC0 SPI1 IO2	SB1V8	OUT HIGH	N.C	GPP H23	GPP H23/TIME SYNC0	SB3V	OUT HIGH	N.C		
GPP D14	GPP D14/THC0 SPI1 IO3	SB1V8	IN	PS2 PINHEADER N	GPP I0	GPP I0/PMCALERT#	SB3V	OUT HIGH	N.C		
GPP D15	GPP D15/SML1DATA	SB1V8	NATIVE	SML1 DATA PCH	GPP I1	GPP I1/DDSP HPD1/DISP MISC1	SB3V	NATIVE	DP DDPC HPD		
GPP D16	GPP D16/GSPI3 CS0#/THC1 SPI2 CS#	SB1V8	OUT HIGH	N.C	GPP I2	GPP I2/DDSP HPD2/DISP MISC2	SB3V	NATIVE	DP DDPC HPD		
GPP D17	GPP D17/GSPI3 CLK/THC1 SPI2 CLK	SB1V8	IN	LPT DET#	GPP I3	GPP I3/DDSP HPD3/DISP MISC3	SB3V	OUT HIGH	N.C		
GPP D18	GPP D18/GSPI3 MISO/THC1 SPI2 IO0	SB1V8	IN	USBDEBUEG	GPP I4	GPP I4/DDSP HPD4/DISP MISC4	SB3V	OUT HIGH	N.C		
GPP D19	GPP D19/GSPI3 MOSI/THC1 SPI2 IO1	SB1V8	OUT HIGH	N.C	GPP I5	GPP I5/DDPB CTRLCLK	SB3V	NATIVE	DP DDPC CTRLCLK		
GPP D20	GPP D20/UART3 RxD/THC1 SPI2 IO2	SB1V8	OUT HIGH	N.C	GPP I6	GPP I6/DDPB CTRLDATA	SB3V	NATIVE	DP DDPC CTRLDATA		
GPP D21	GPP D21/UART3 TXD/THC1 SPI2 IO3	SB1V8	OUT HIGH	N.C	GPP I7	GPP I7/DDPC CTRLCLK	SB3V	OUT HIGH	N.C		
GPP D22	GPP D22/UART3 RTS#/THC1 SPI2 RST#	SB1V8	OUT HIGH	N.C	GPP I8	GPP I8/DDPC CTRLDATA	SB3V	NATIVE	DPC CTRLDATA		
GPP D23	GPP D23/UART3 CTS#/THC1 SPI2 INT#	SB1V8	OUT HIGH	N.C	GPP I9	GPP I9	SB3V	OUT HIGH	N.C		
					GPP I10	GPP I10	SB3V	OUT HIGH	N.C		



